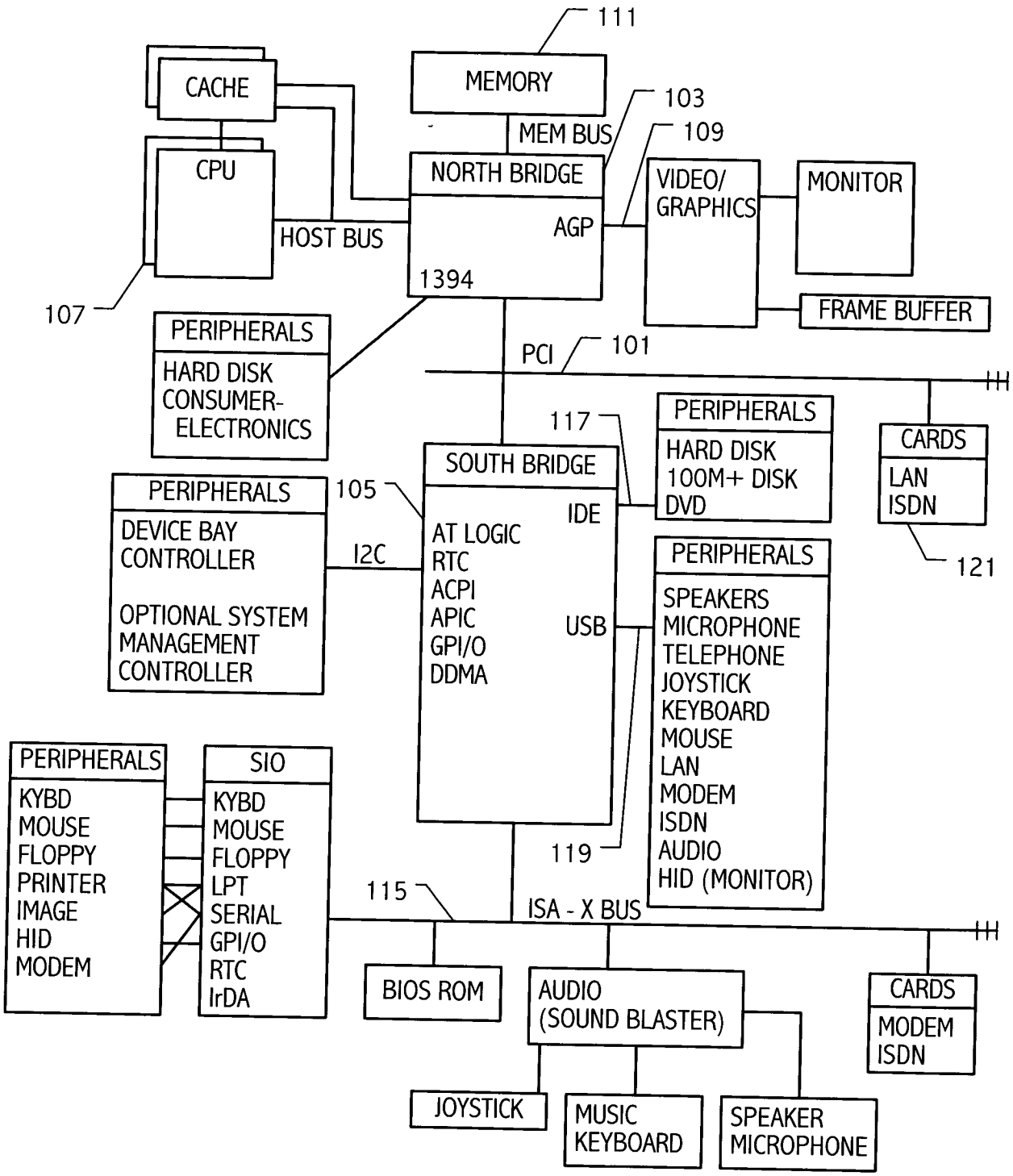

FIG. 1
(Prior Art)

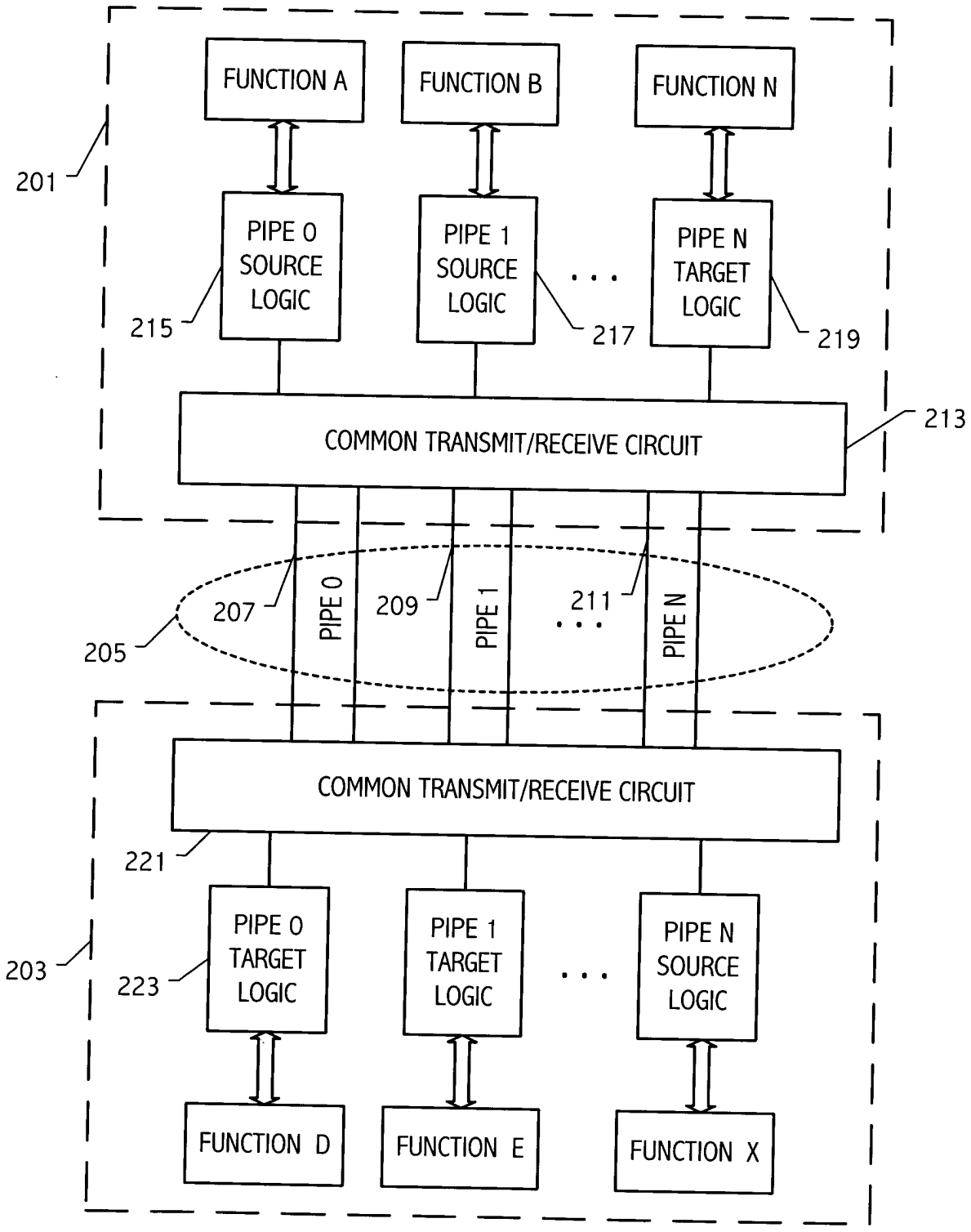
FUNCTION A
FUNCTION B
FUNCTION N
201
PIPE 0 SOURCE LOGIC
PIPE 1 SOURCE LOGIC
PIPE N TARGET LOGIC
215
217
219
COMMON TRANSMIT/RECEIVE CIRCUIT
213
207
PIPE 0
209
PIPE 1
211
PIPE N
205
COMMON TRANSMIT/RECEIVE CIRCUIT
221
203
223
PIPE 0 TARGET LOGIC
PIPE 1 TARGET LOGIC
PIPE N SOURCE LOGIC
FUNCTION D
FUNCTION E
FUNCTION X

FIG. 2

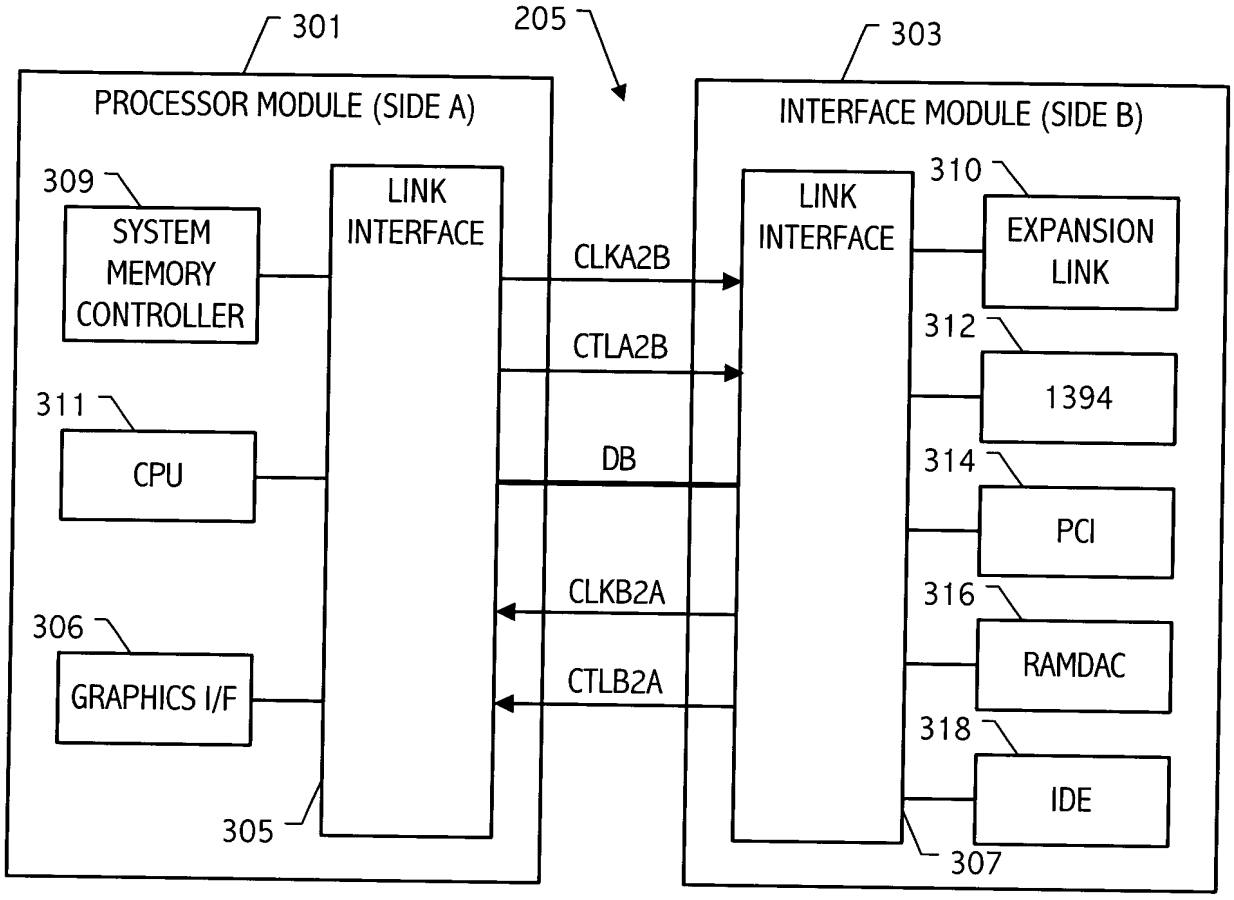
301
205
303
PROCESSOR MODULE (SIDE A)
INTERFACE MODULE (SIDE B)
309
SYSTEM MEMORY CONTROLLER
LINK INTERFACE
LINK INTERFACE
310
EXPANSION LINK
CLKA2B
CTLA2B
312
1394
311
CPU
DB
314
PCI
CLKB2A
316
306
GRAPHICS I/F
RAMDAC
CTLB2A
318
IDE
305
307

FIG. 3

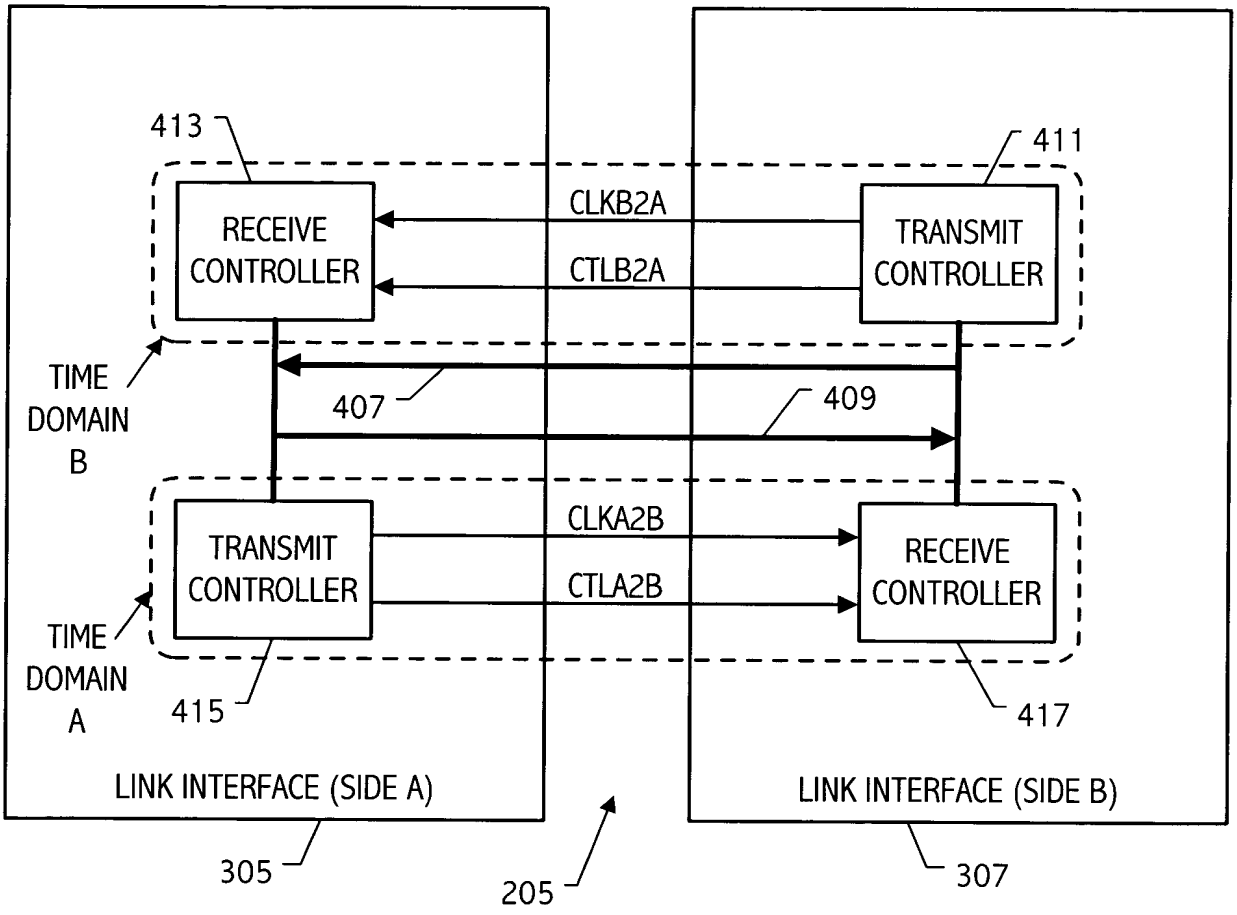
413
411
RECEIVE CONTROLLER
CLKB2A
CTLB2A
TRANSMIT CONTROLLER
TIME DOMAIN B
407
409
TRANSMIT CONTROLLER
CLKA2B
CTLA2B
RECEIVE CONTROLLER
TIME DOMAIN A
415
417
LINK INTERFACE (SIDE A)
LINK INTERFACE (SIDE B)
305
205
307

FIG. 4

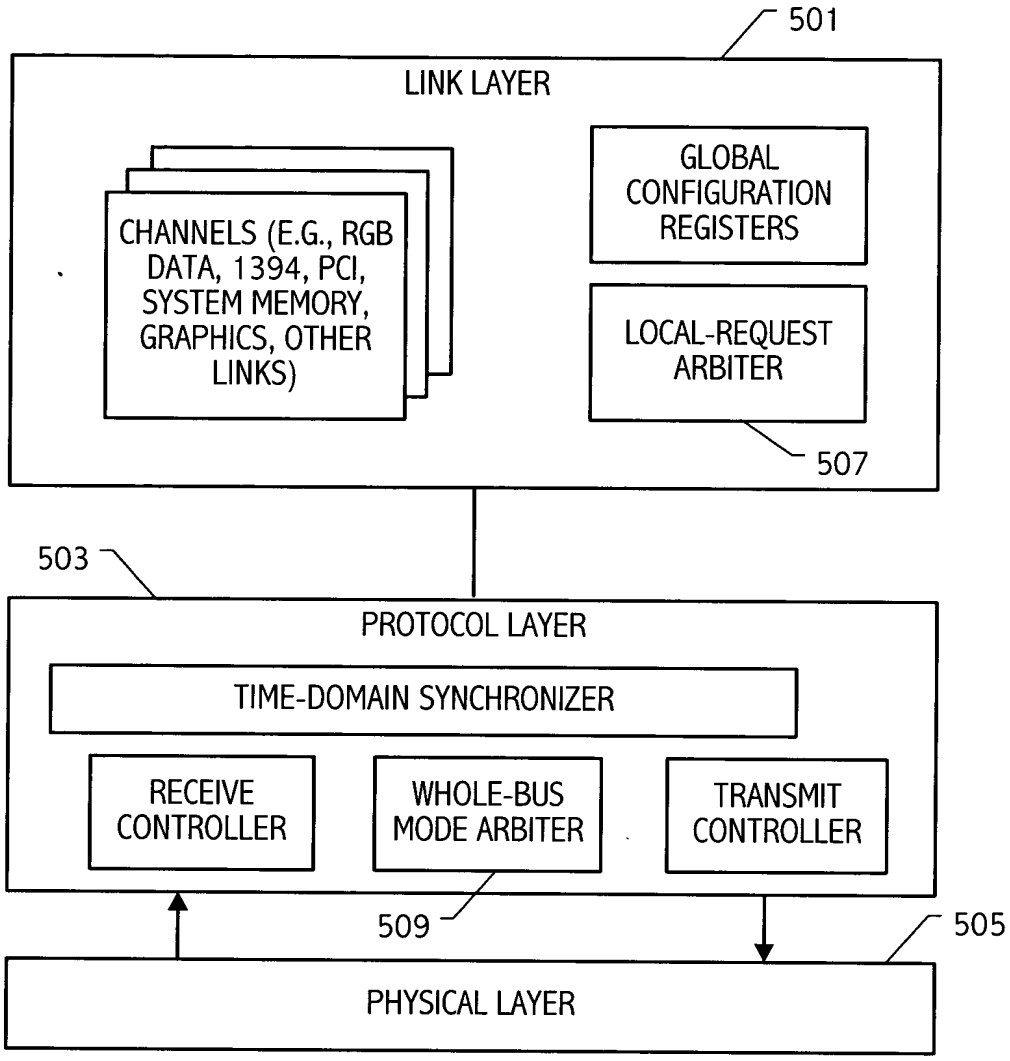

FIG. 5

START	END	NAME	DESCRIPTION
FE 0200 0000	FE FFFF FFFF	RESERVED	
FE 0100 0000	FE 01FF FFFF	CONFIGURATION	24-BIT CONFIGURATION SPACE
FE 0001 0000	FE 00FF FFFF	RESERVED	
FE 0000 0000	FE 0000 FFFF	x86 I/O	16-BIT x86 I/O ADDRESS SPACE
00 0000 0000	FD FFFF F FFF	NORMAL MEMORY	DRAM ADDRESS SPACE
00 0000 0000	00 FFFF FFFF	PCI MEMORY	32-BIT PCI ADDRESS SPACE

FIG. 6

MEMORY WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)	DATA (1-64)

FIG. 7A

SPECIAL CYCLE WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)	DATA (4)

FIG. 7B

NON-ADDRESSED WRITE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	RSRVD (2)	SIZE (6)	DATA (1-64)

FIG. 7C

WRITE ACK (OR NAK) PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)

FIG. 7D

FLUSH PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)

FIG. 7E

FENCE PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)

FIG. 7F

MEMORY READ REQUEST PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	ADDR (40)	RSRVD (2)	SIZE (6)

FIG. 7G

NON-ADDRESSED READ REQUE ST PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (1)	BUF AVAIL (4)	RSRVD (2)	SIZE (6)

FIG. 7H

READ RESPONSE PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)	RSRVD (2)	SIZE (6)	DATA (1-64)

FIG. 7I

NON-ADDRESSED READ R ESPONSE PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (1)	BUF AVAIL (4)	RSRVD (2)	SIZE (6)	DATA (1-64)

FIG. 7J

READ REJECT PACKET

PIPE ID # (5)	PKT TYPE (6)	TAG (5)	BUF AVAIL (4)	RSRVD (4)

FIG. 7K

NOP PACKET

PIPE ID # (5)	PKT TYPE (6)	RSRVD (5)	BUF AVAIL (4)	RSRVD (4)

FIG. 7L

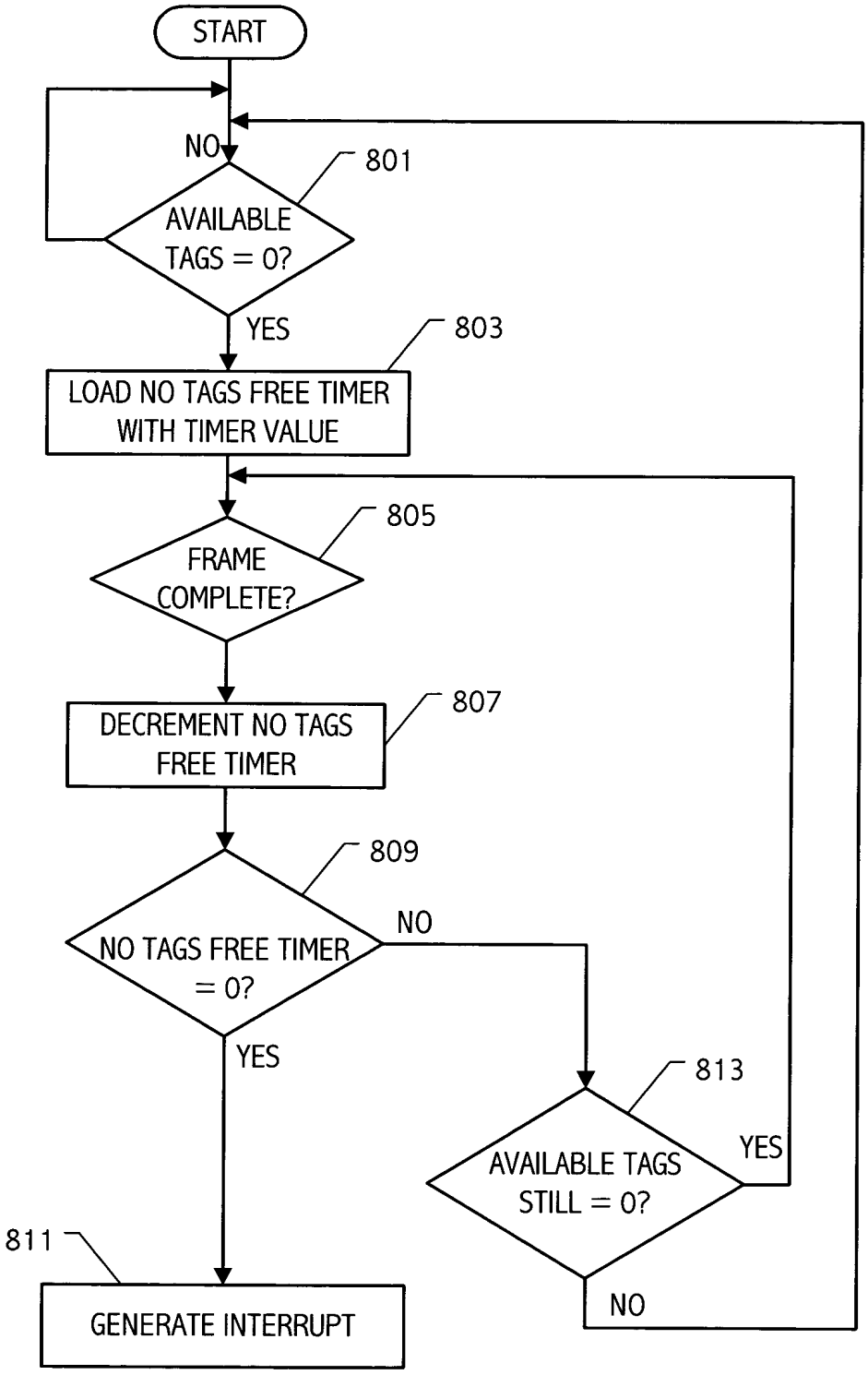
START
NO
801
AVAILABLE TAGS = 0?
YES
803
LOAD NO TAGS FREE TIMER WITH TIMER VALUE
805
FRAME COMPLETE?
807
DECREMENT NO TAGS FREE TIMER
809
NO TAGS FREE TIMER = 0?
NO
YES
813
AVAILABLE TAGS STILL = 0?
YES
NO
811
GENERATE INTERRUPT

FIG. 8

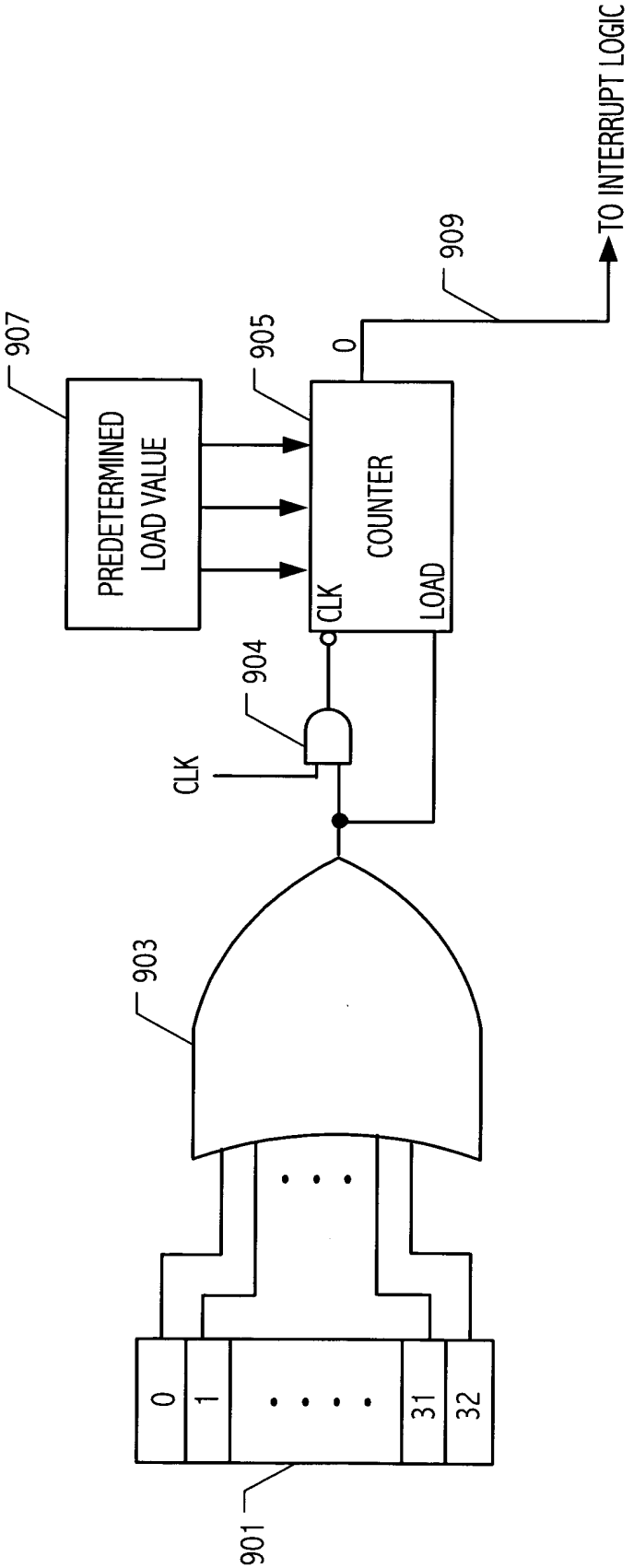
TO INTERRUPT LOGIC
909
907
905
0
PREDETERMINED LOAD VALUE
COUNTER
CLK
LOAD
904
CLK
903
0
1
31
32
901

FIG. 9

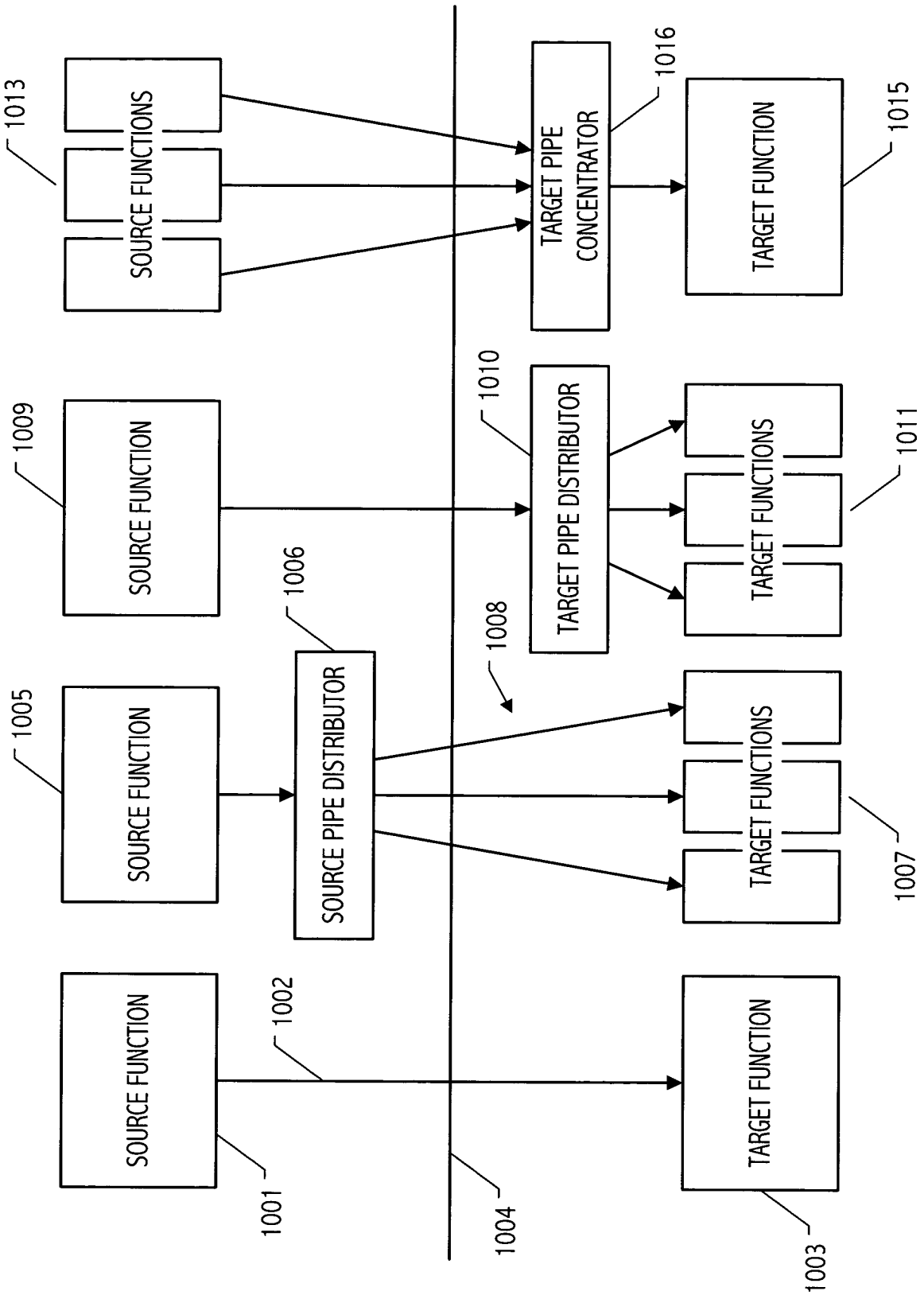
SOURCE FUNCTION
1001
1002
TARGET FUNCTION
1003
1004
SOURCE FUNCTION
1005
SOURCE PIPE DISTRIBUTOR
1006
TARGET FUNCTIONS
1007
1008
SOURCE FUNCTION
1009
TARGET PIPE DISTRIBUTOR
1010
TARGET FUNCTIONS
1011
SOURCE FUNCTIONS
1013
TARGET PIPE CONCENTRATOR
1016
TARGET FUNCTION
1015

FIG. 10

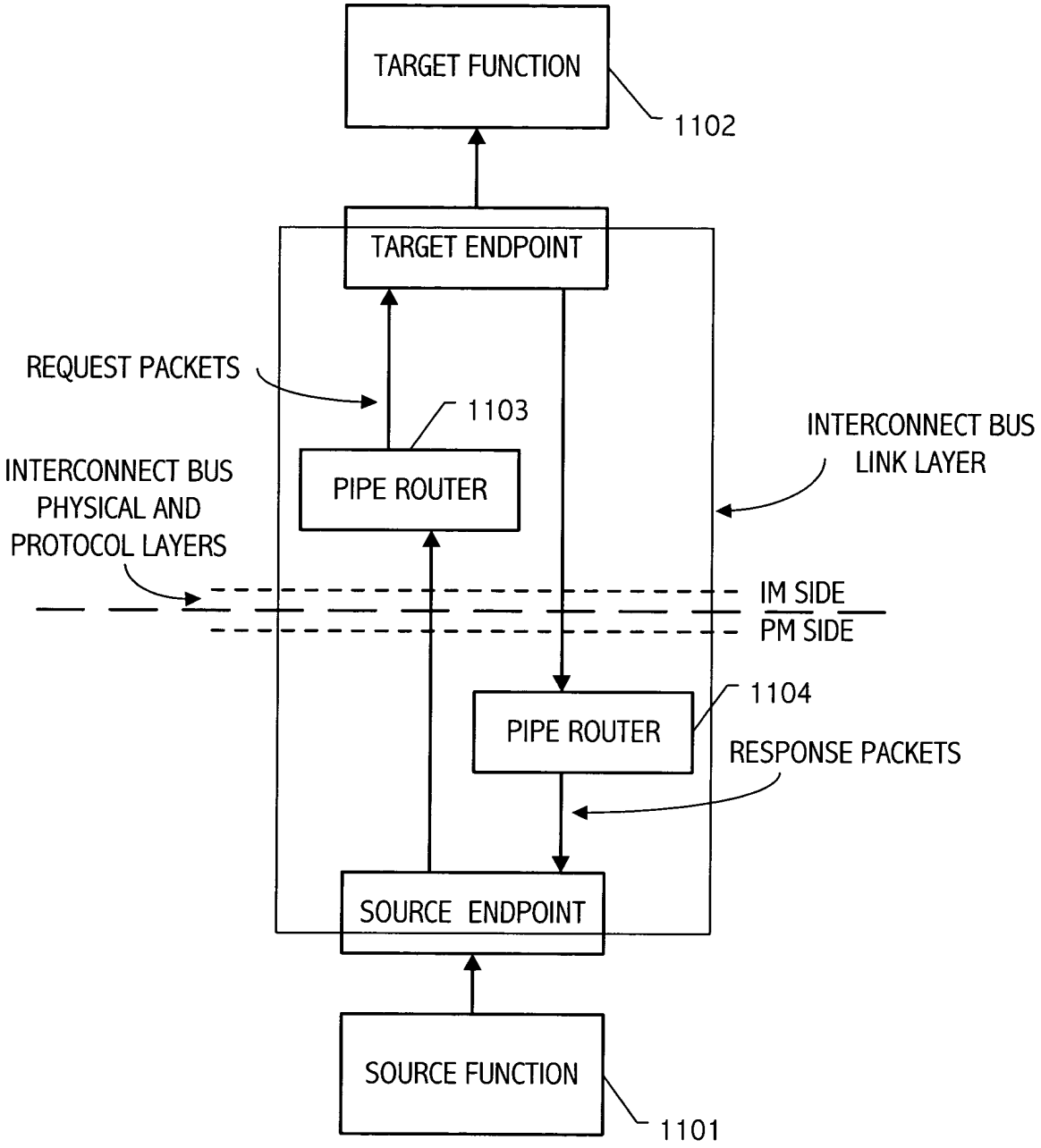
TARGET FUNCTION
1102
TARGET ENDPOINT
REQUEST PACKETS
1103
INTERCONNECT BUS
LINK LAYER
INTERCONNECT BUS
PHYSICAL AND
PROTOCOL LAYERS
PIPE ROUTER
IM SIDE
PM SIDE
1104
PIPE ROUTER
RESPONSE PACKETS
SOURCE ENDPOINT
SOURCE FUNCTION
1101

FIG. 11

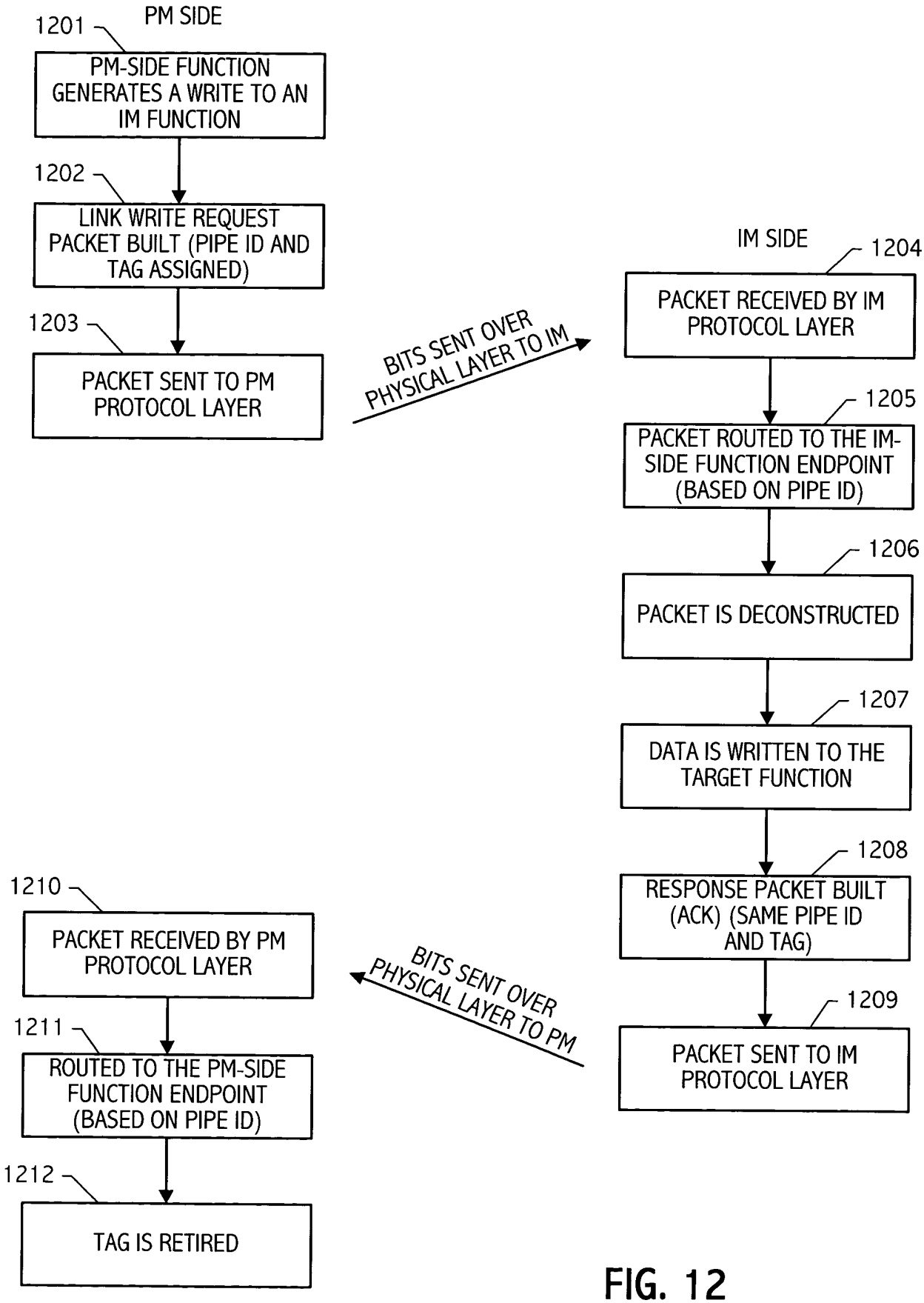
PM SIDE
1201
PM-SIDE FUNCTION GENERATES A WRITE TO AN IM FUNCTION
1202
LINK WRITE REQUEST PACKET BUILT (PIPE ID AND TAG ASSIGNED)
1203
PACKET SENT TO PM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO IM
IM SIDE
1204
PACKET RECEIVED BY IM PROTOCOL LAYER
1205
PACKET ROUTED TO THE IM-SIDE FUNCTION ENDPOINT (BASED ON PIPE ID)
1206
PACKET IS DECONSTRUCTED
1207
DATA IS WRITTEN TO THE TARGET FUNCTION
1208
RESPONSE PACKET BUILT (ACK) (SAME PIPE ID AND TAG)
1209
PACKET SENT TO IM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO PM
1210
PACKET RECEIVED BY PM PROTOCOL LAYER
1211
ROUTED TO THE PM-SIDE FUNCTION ENDPOINT (BASED ON PIPE ID)
1212
TAG IS RETIRED

FIG. 12

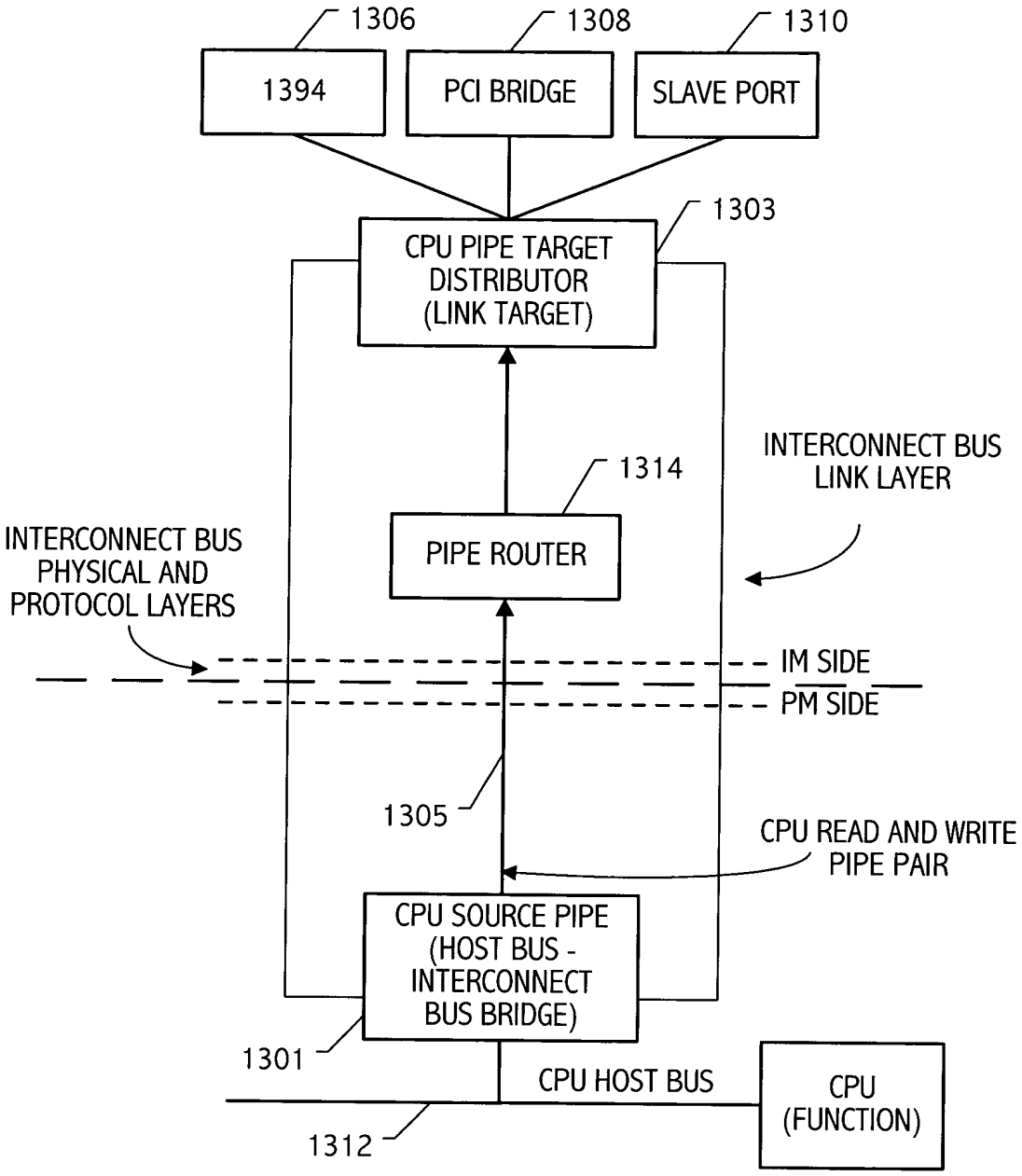
1306
1308
1310
1394
PCI BRIDGE
SLAVE PORT
1303
CPU PIPE TARGET DISTRIBUTOR (LINK TARGET)
INTERCONNECT BUS LINK LAYER
1314
PIPE ROUTER
INTERCONNECT BUS PHYSICAL AND PROTOCOL LAYERS
IM SIDE
PM SIDE
1305
CPU READ AND WRITE PIPE PAIR
CPU SOURCE PIPE (HOST BUS - INTERCONNECT BUS BRIDGE)
1301
CPU HOST BUS
CPU (FUNCTION)
1312

FIG. 13

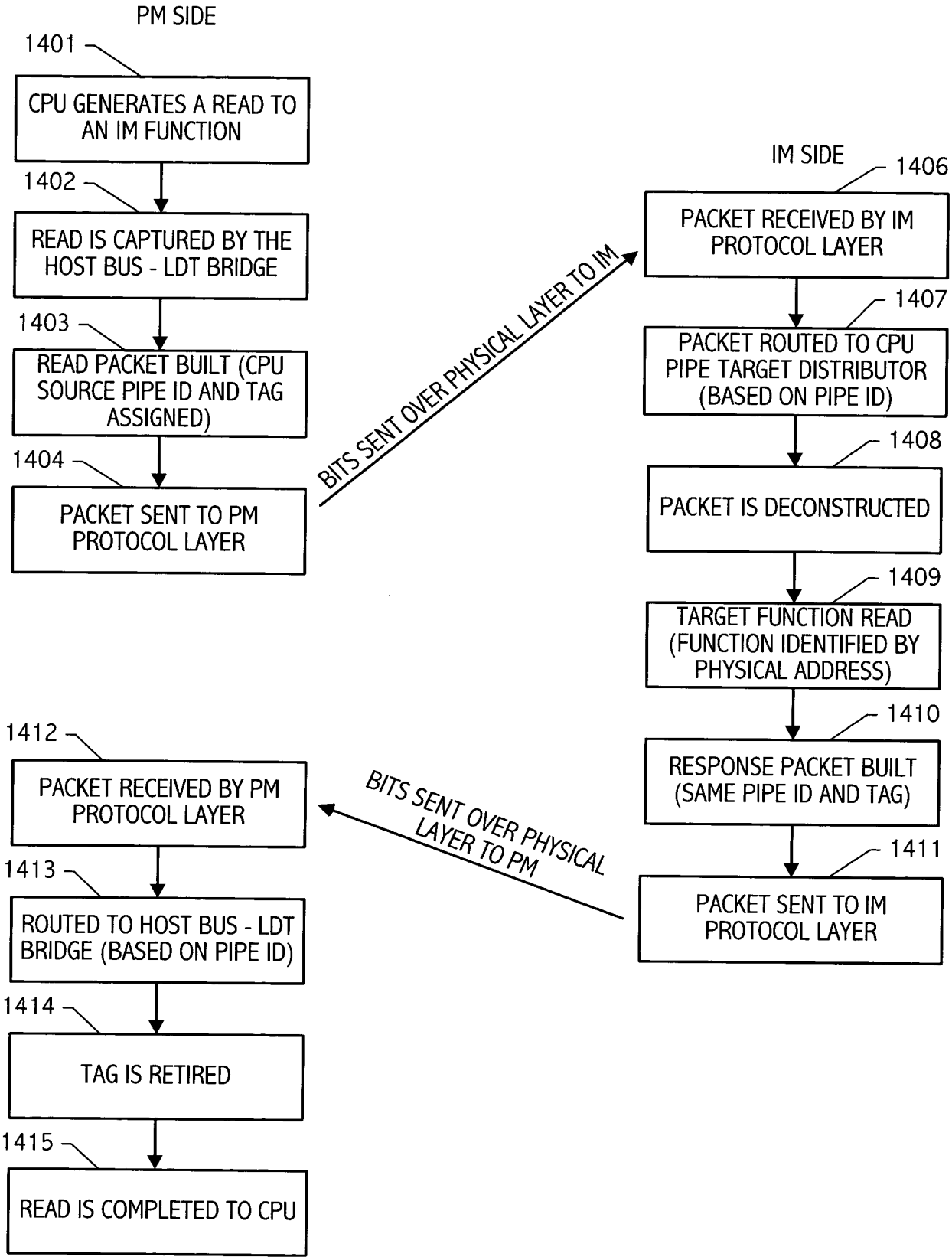
PM SIDE
1401
CPU GENERATES A READ TO AN IM FUNCTION
1402
READ IS CAPTURED BY THE HOST BUS - LDT BRIDGE
1403
READ PACKET BUILT (CPU SOURCE PIPE ID AND TAG ASSIGNED)
1404
PACKET SENT TO PM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO IM
IM SIDE
1406
PACKET RECEIVED BY IM PROTOCOL LAYER
1407
PACKET ROUTED TO CPU PIPE TARGET DISTRIBUTOR (BASED ON PIPE ID)
1408
PACKET IS DECONSTRUCTED
1409
TARGET FUNCTION READ (FUNCTION IDENTIFIED BY PHYSICAL ADDRESS)
1410
RESPONSE PACKET BUILT (SAME PIPE ID AND TAG)
1411
PACKET SENT TO IM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO PM
1412
PACKET RECEIVED BY PM PROTOCOL LAYER
1413
ROUTED TO HOST BUS - LDT BRIDGE (BASED ON PIPE ID)
1414
TAG IS RETIRED
1415
READ IS COMPLETED TO CPU

FIG. 14

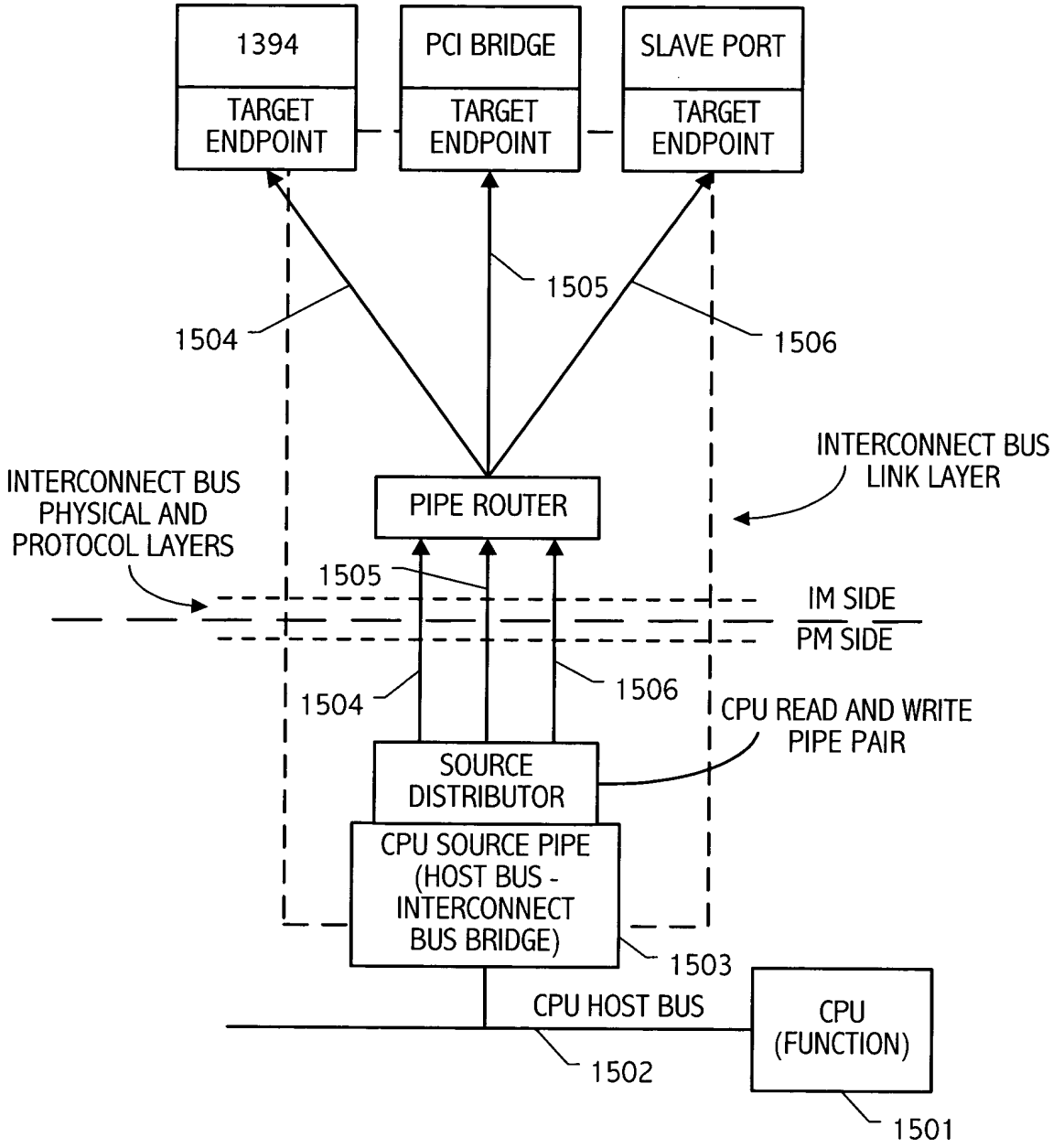
1394
TARGET ENDPOINT
PCI BRIDGE
TARGET ENDPOINT
SLAVE PORT
TARGET ENDPOINT
1504
1505
1506
INTERCONNECT BUS LINK LAYER
INTERCONNECT BUS PHYSICAL AND PROTOCOL LAYERS
PIPE ROUTER
1505
IM SIDE
PM SIDE
1504
1506
CPU READ AND WRITE PIPE PAIR
SOURCE DISTRIBUTOR
CPU SOURCE PIPE (HOST BUS - INTERCONNECT BUS BRIDGE)
1503
CPU HOST BUS
CPU (FUNCTION)
1502
1501

FIG.15

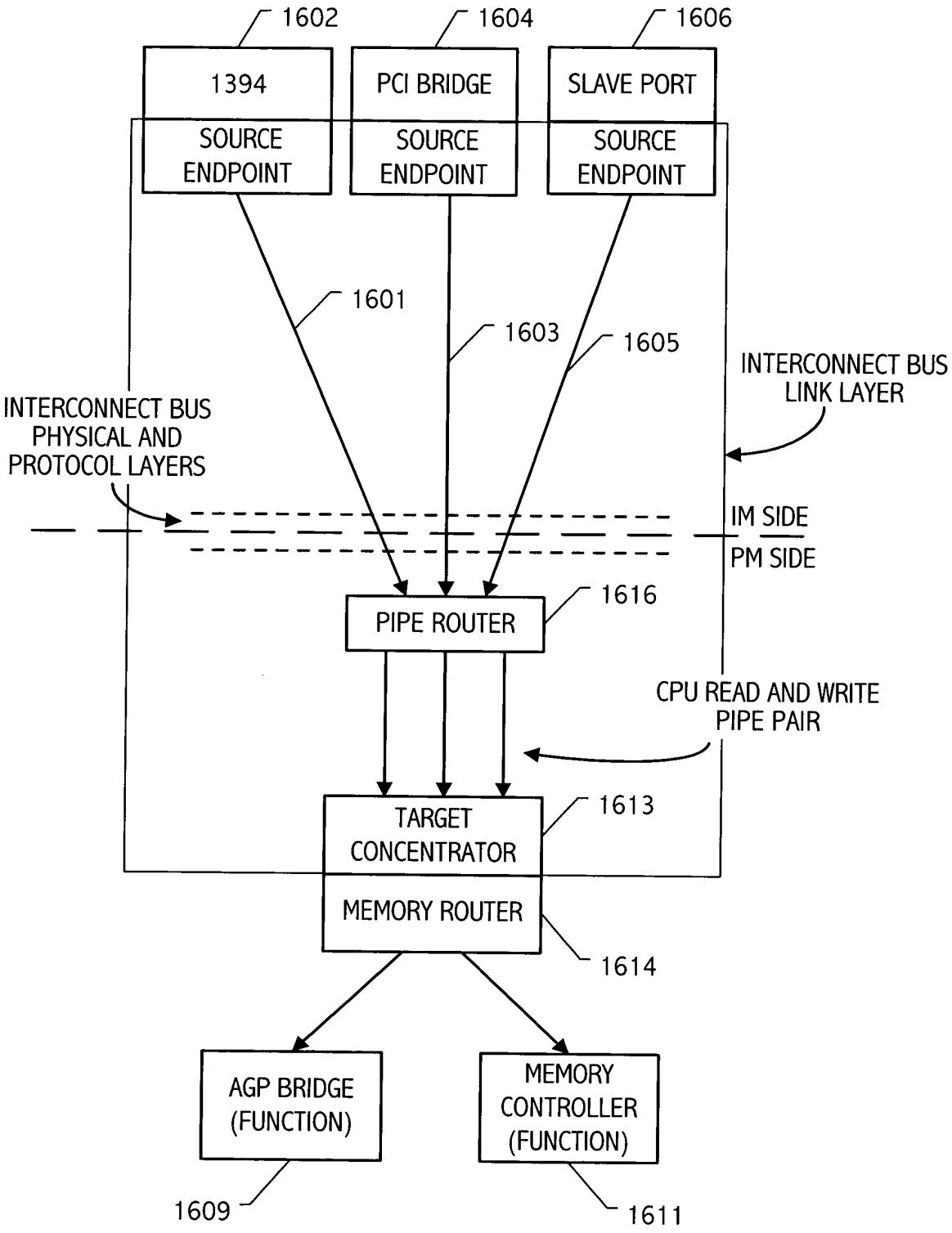
1602
1604
1606
1394
PCI BRIDGE
SLAVE PORT
SOURCE ENDPOINT
SOURCE ENDPOINT
SOURCE ENDPOINT
1601
1603
1605
INTERCONNECT BUS LINK LAYER
INTERCONNECT BUS PHYSICAL AND PROTOCOL LAYERS
IM SIDE
PM SIDE
PIPE ROUTER
1616
CPU READ AND WRITE PIPE PAIR
TARGET CONCENTRATOR
1613
MEMORY ROUTER
1614
AGP BRIDGE (FUNCTION)
MEMORY CONTROLLER (FUNCTION)
1609
1611

FIG. 16

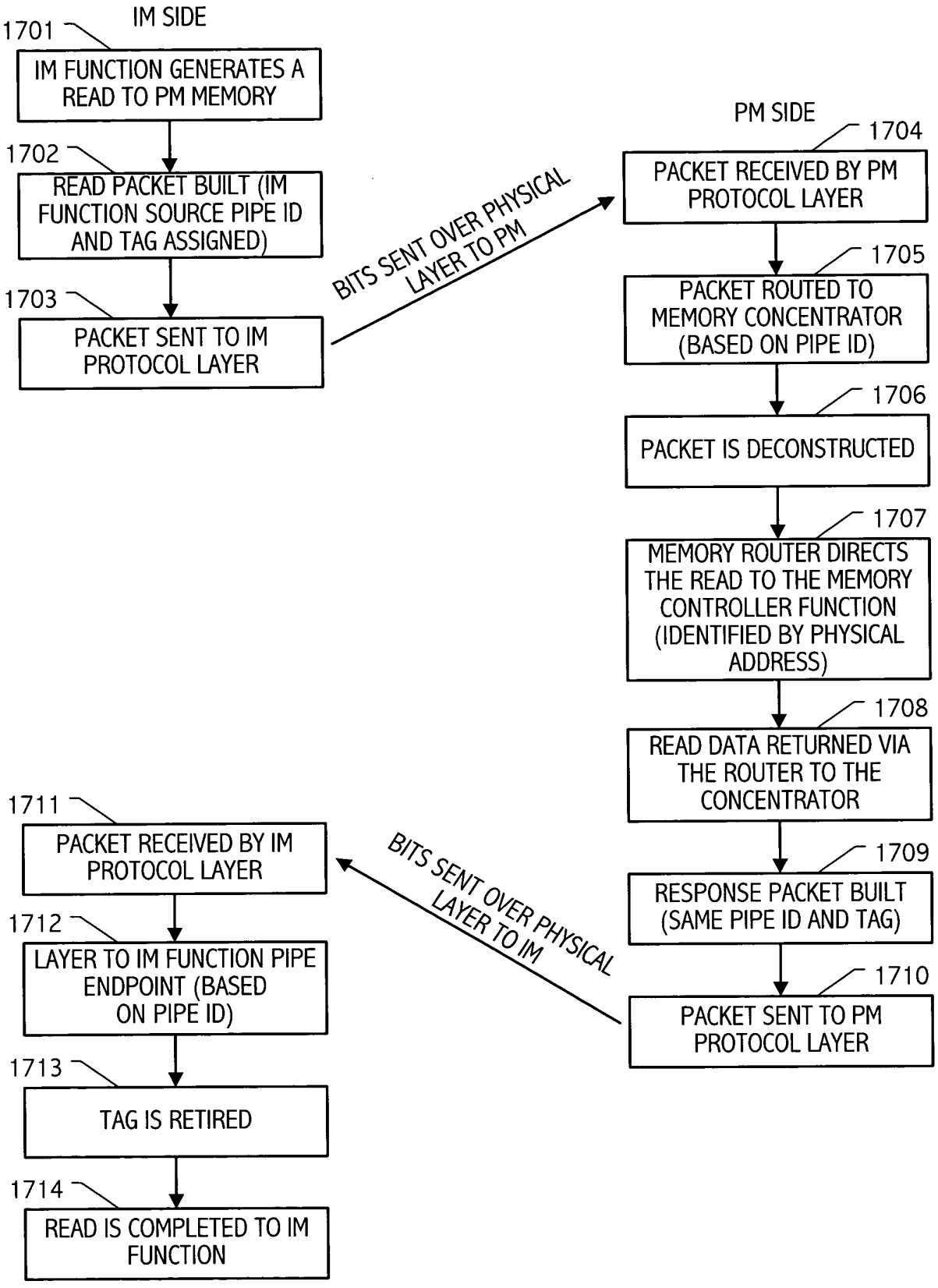
IM SIDE
1701
IM FUNCTION GENERATES A READ TO PM MEMORY
1702
READ PACKET BUILT (IM FUNCTION SOURCE PIPE ID AND TAG ASSIGNED)
1703
PACKET SENT TO IM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO PM
PM SIDE
1704
PACKET RECEIVED BY PM PROTOCOL LAYER
1705
PACKET ROUTED TO MEMORY CONCENTRATOR (BASED ON PIPE ID)
1706
PACKET IS DECONSTRUCTED
1707
MEMORY ROUTER DIRECTS THE READ TO THE MEMORY CONTROLLER FUNCTION (IDENTIFIED BY PHYSICAL ADDRESS)
1708
READ DATA RETURNED VIA THE ROUTER TO THE CONCENTRATOR
1709
RESPONSE PACKET BUILT (SAME PIPE ID AND TAG)
1710
PACKET SENT TO PM PROTOCOL LAYER
BITS SENT OVER PHYSICAL LAYER TO IM
1711
PACKET RECEIVED BY IM PROTOCOL LAYER
1712
LAYER TO IM FUNCTION PIPE ENDPOINT (BASED ON PIPE ID)
1713
TAG IS RETIRED
1714
READ IS COMPLETED TO IM FUNCTION

FIG. 17

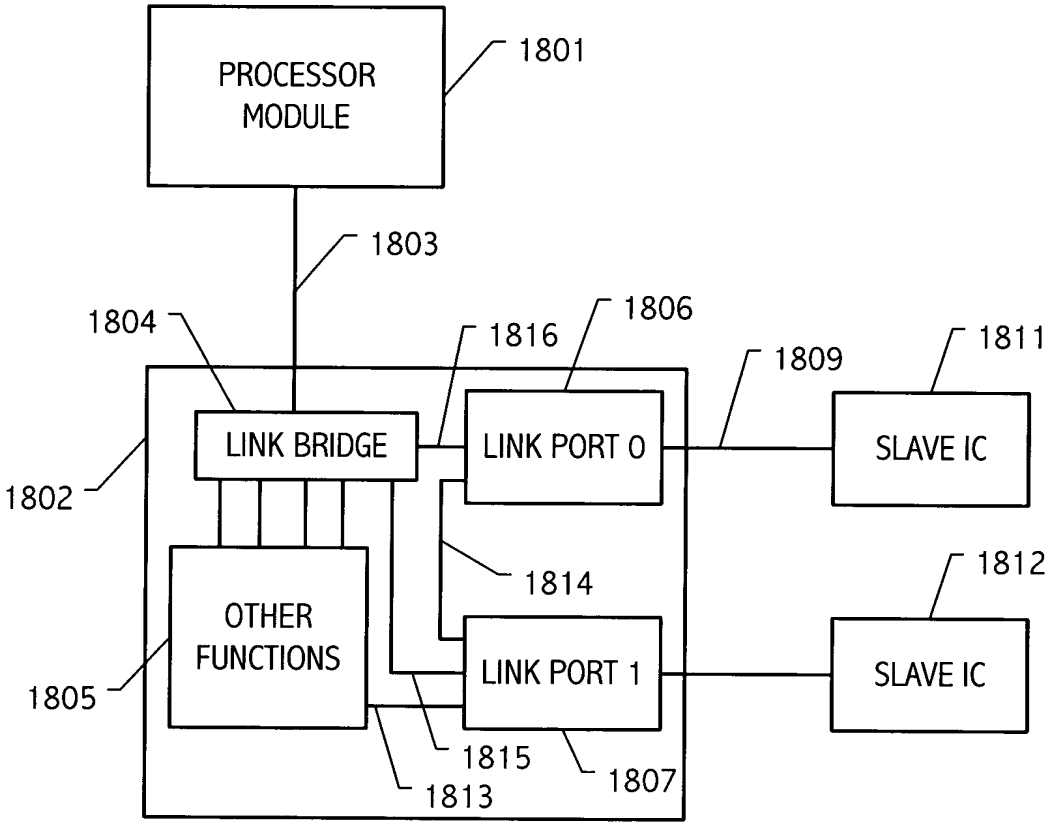
PROCESSOR MODULE
1801
1803
1804
1816
1806
1809
1811
LINK BRIDGE
LINK PORT 0
SLAVE IC
1802
1814
1812
OTHER FUNCTIONS
LINK PORT 1
SLAVE IC
1805
1815
1807
1813

FIG. 18

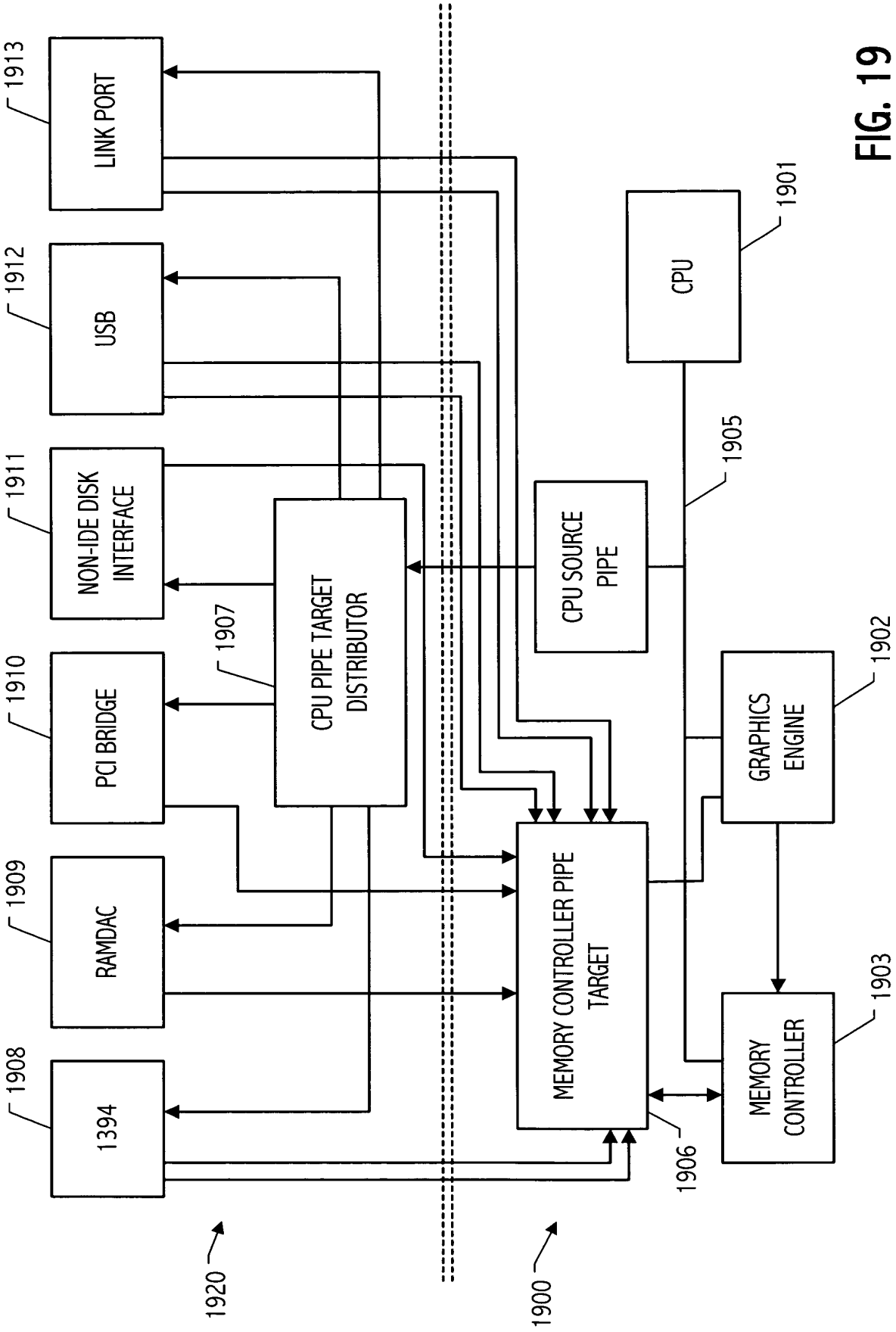
1913
LINK PORT
1912
USB
1911
NON-IDE DISK INTERFACE
1910
PCI BRIDGE
1909
RAMDAC
1908
1394
1907
CPU PIPE TARGET DISTRIBUTOR
CPU SOURCE PIPE
1905
CPU
1901
GRAPHICS ENGINE
1902
MEMORY CONTROLLER PIPE TARGET
MEMORY CONTROLLER
1903
1906
1920
1900

FIG. 19

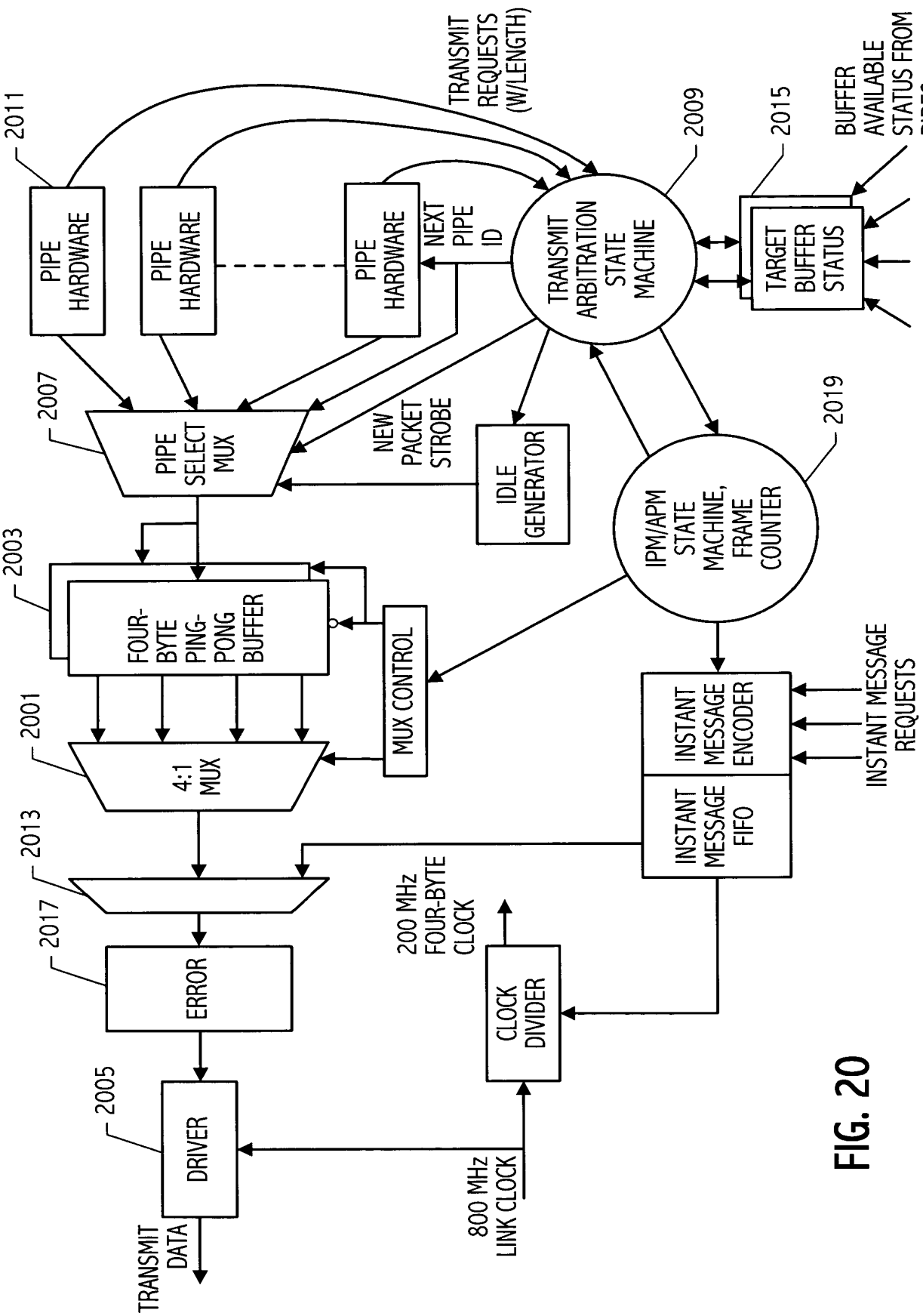
2011
PIPE HARDWARE
PIPE HARDWARE
PIPE HARDWARE
NEXT PIPE ID
TRANSMIT REQUESTS (W/LENGTH)
2009
TRANSMIT ARBITRATION STATE MACHINE
2015
TARGET BUFFER STATUS
BUFFER AVAILABLE STATUS FROM PIPES
2007
PIPE SELECT MUX
NEW PACKET STROBE
IDLE GENERATOR
2019
IPM/APM STATE MACHINE, FRAME COUNTER
2003
FOUR-BYTE PING-PONG BUFFER
MUX CONTROL
2001
4:1 MUX
INSTANT MESSAGE ENCODER
INSTANT MESSAGE FIFO
INSTANT MESSAGE REQUESTS
2013
2017
ERROR
200 MHz FOUR-BYTE CLOCK
CLOCK DIVIDER
2005
DRIVER
800 MHz LINK CLOCK
TRANSMIT DATA

FIG. 20

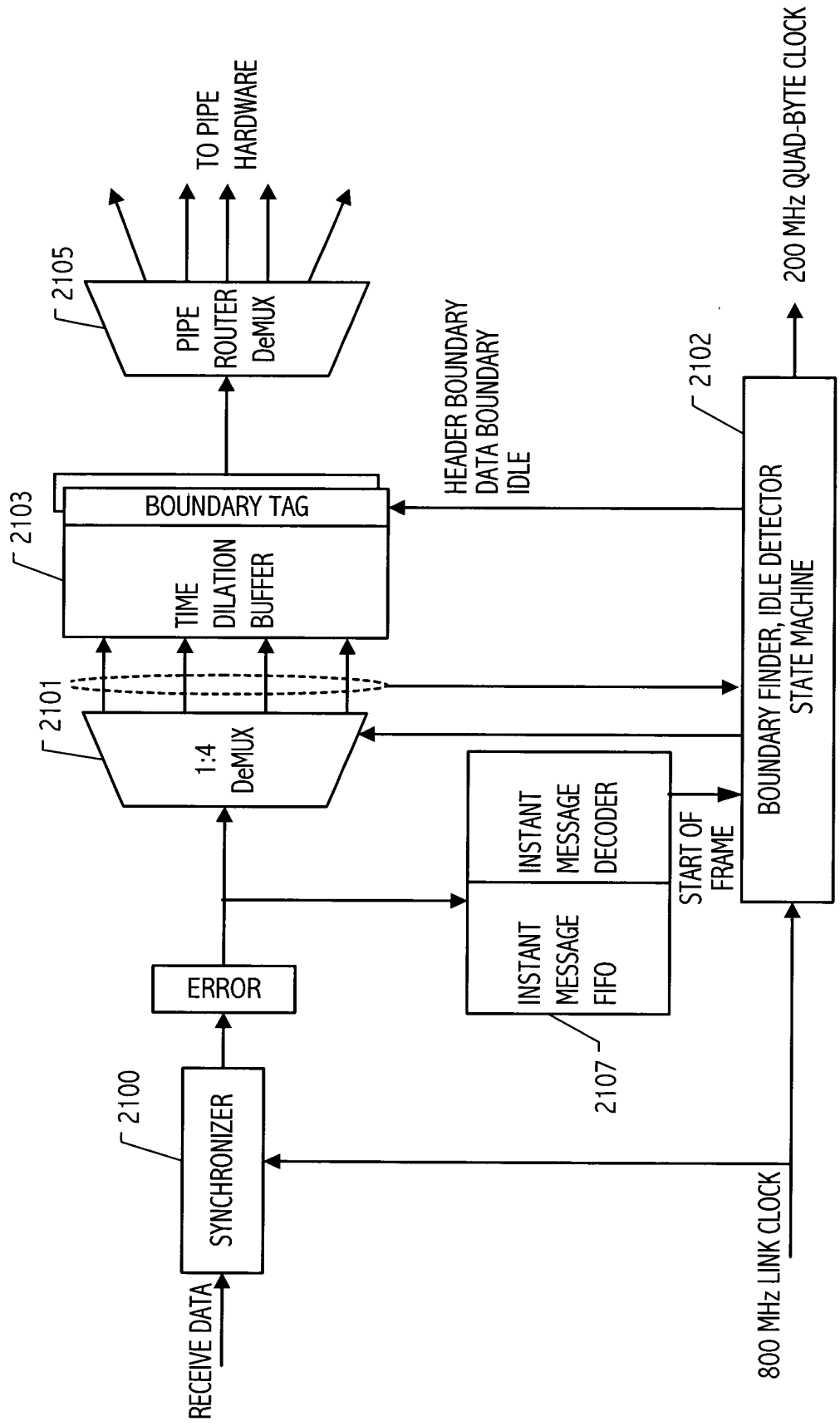
TO PIPE HARDWARE
2105
PIPE ROUTER DeMUX
HEADER BOUNDARY
DATA BOUNDARY
IDLE
200 MHz QUAD-BYTE CLOCK
2102
2103
BOUNDARY TAG
TIME DILATION BUFFER
BOUNDARY FINDER, IDLE DETECTOR STATE MACHINE
2101
1:4 DeMUX
INSTANT MESSAGE DECODER
START OF FRAME
ERROR
INSTANT MESSAGE FIFO
2107
2100
SYNCHRONIZER
RECEIVE DATA
800 MHz LINK CLOCK

FIG. 21

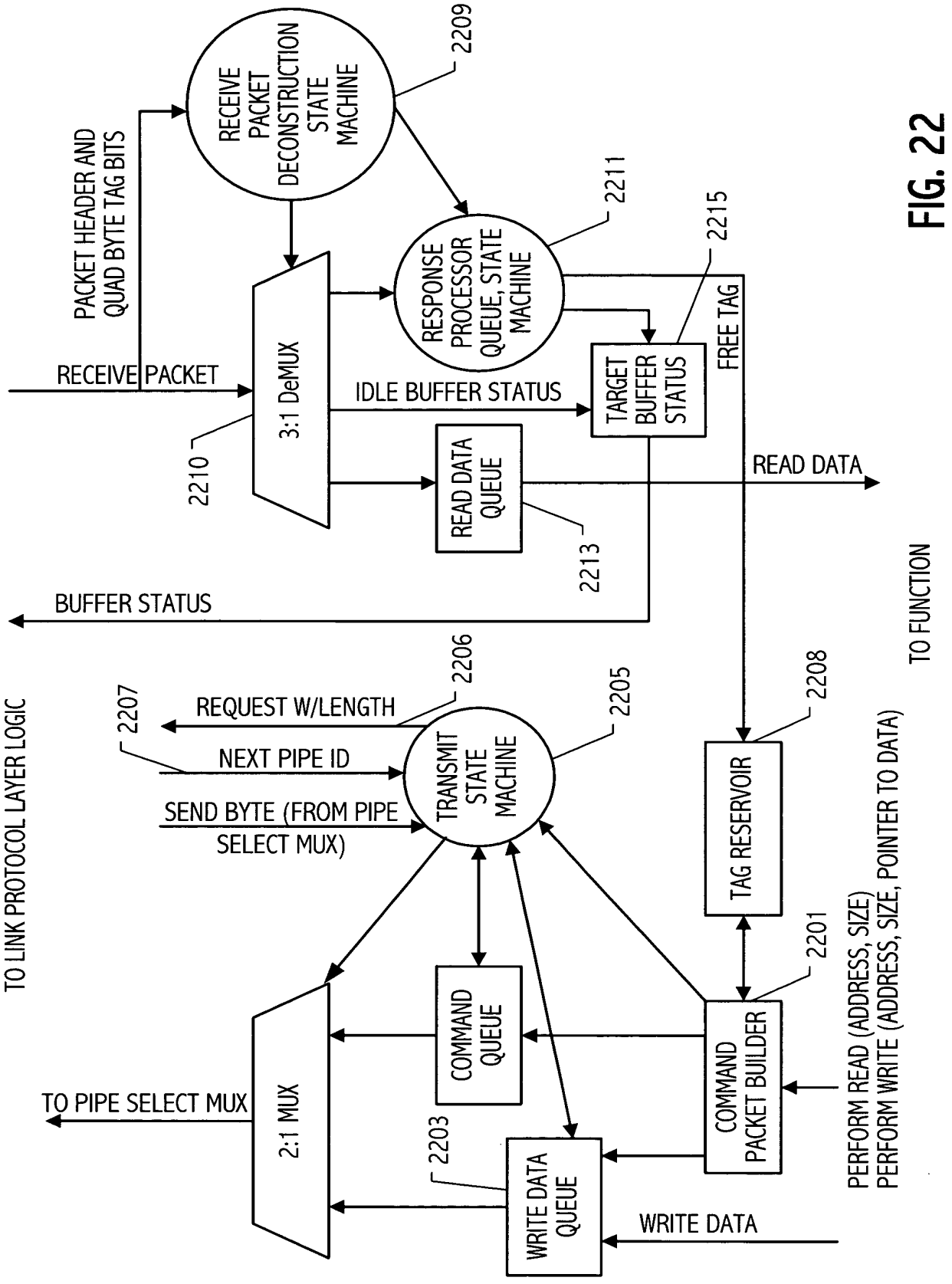
RECEIVE PACKET DECONSTRUCTION STATE MACHINE
2209
PACKET HEADER AND QUAD BYTE TAG BITS
RECEIVE PACKET
3:1 DeMUX
2210
RESPONSE PROCESSOR QUEUE, STATE MACHINE
2211
2215
FREE TAG
IDLE BUFFER STATUS
TARGET BUFFER STATUS
READ DATA QUEUE
2213
READ DATA
BUFFER STATUS
TO FUNCTION
TO LINK PROTOCOL LAYER LOGIC
2207
REQUEST W/LENGTH
2206
NEXT PIPE ID
SEND BYTE (FROM PIPE SELECT MUX)
TRANSMIT STATE MACHINE
2205
2208
TAG RESERVOIR
2201
COMMAND QUEUE
COMMAND PACKET BUILDER
PERFORM READ (ADDRESS, SIZE)
PERFORM WRITE (ADDRESS, SIZE, POINTER TO DATA)
TO PIPE SELECT MUX
2:1 MUX
2203
WRITE DATA QUEUE
WRITE DATA

FIG. 22

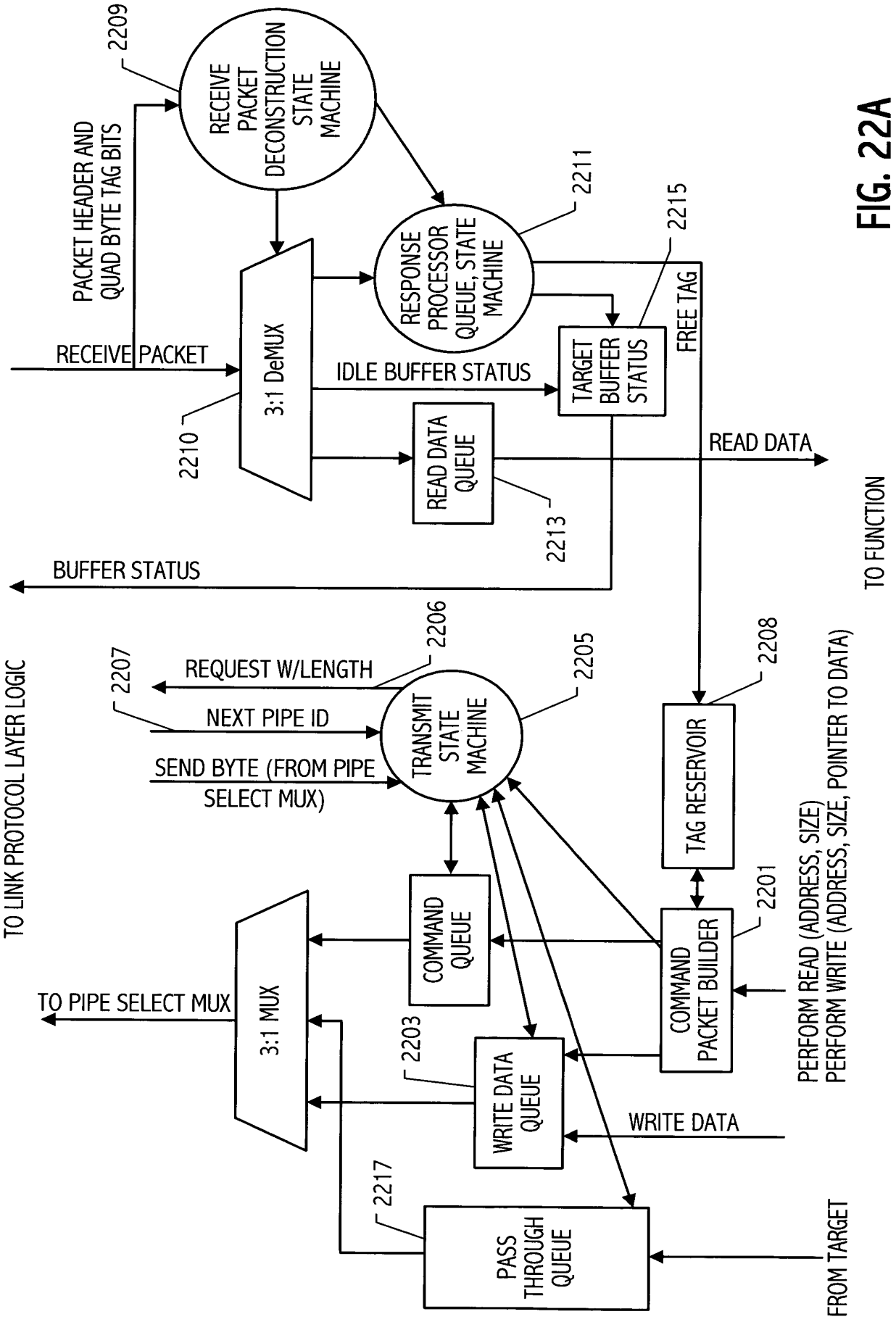
2209
RECEIVE PACKET DECONSTRUCTION STATE MACHINE
PACKET HEADER AND QUAD BYTE TAG BITS
2211
RESPONSE PROCESSOR QUEUE, STATE MACHINE
2215
FREE TAG
RECEIVE PACKET
3:1 DeMUX
IDLE BUFFER STATUS
TARGET BUFFER STATUS
2210
READ DATA QUEUE
READ DATA
2213
BUFFER STATUS
TO FUNCTION
TO LINK PROTOCOL LAYER LOGIC
2207
REQUEST W/LENGTH
2206
2205
NEXT PIPE ID
SEND BYTE (FROM PIPE SELECT MUX)
TRANSMIT STATE MACHINE
2208
TAG RESERVOIR
2201
COMMAND QUEUE
COMMAND PACKET BUILDER
PERFORM READ (ADDRESS, SIZE)
PERFORM WRITE (ADDRESS, SIZE, POINTER TO DATA)
TO PIPE SELECT MUX
3:1 MUX
2203
WRITE DATA QUEUE
WRITE DATA
2217
PASS THROUGH QUEUE
FROM TARGET

FIG. 22A

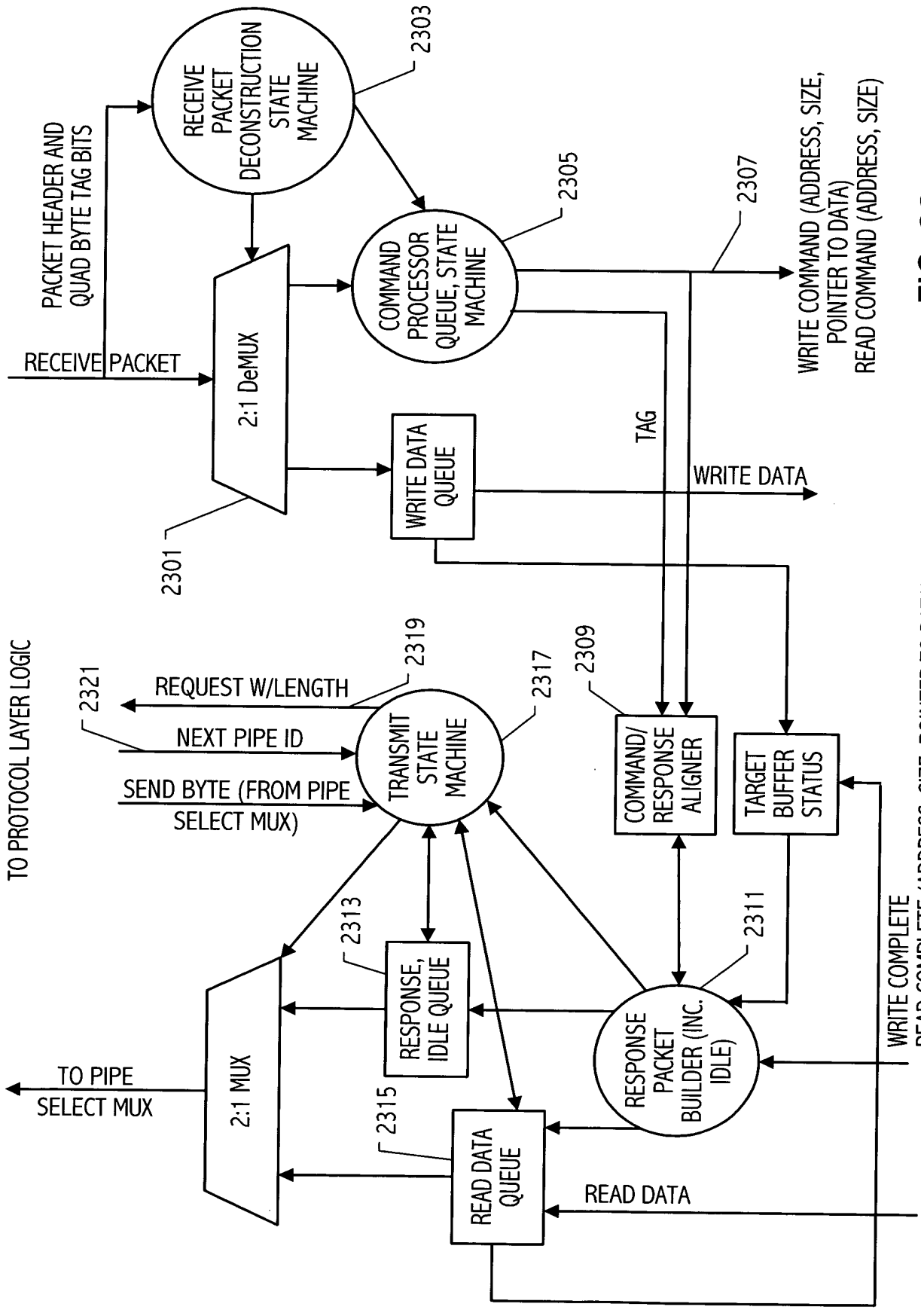
RECEIVE PACKET DECONSTRUCTION STATE MACHINE
2303
PACKET HEADER AND QUAD BYTE TAG BITS
RECEIVE PACKET
2:1 DeMUX
2301
COMMAND PROCESSOR QUEUE, STATE MACHINE
2305
2307
WRITE COMMAND (ADDRESS, SIZE, POINTER TO DATA)
READ COMMAND (ADDRESS, SIZE)
TAG
WRITE DATA QUEUE
WRITE DATA
TO FUNCTION
TO PROTOCOL LAYER LOGIC
2321
REQUEST W/LENGTH
NEXT PIPE ID
SEND BYTE (FROM PIPE SELECT MUX)
TRANSMIT STATE MACHINE
2319
2317
2309
COMMAND/ RESPONSE ALIGNER
TARGET BUFFER STATUS
2313
RESPONSE, IDLE QUEUE
2311
TO PIPE SELECT MUX
2:1 MUX
RESPONSE PACKET BUILDER (INC. IDLE)
WRITE COMPLETE
READ COMPLETE (ADDRESS, SIZE, POINTER TO DATA)
2315
READ DATA QUEUE
READ DATA

FIG. 23

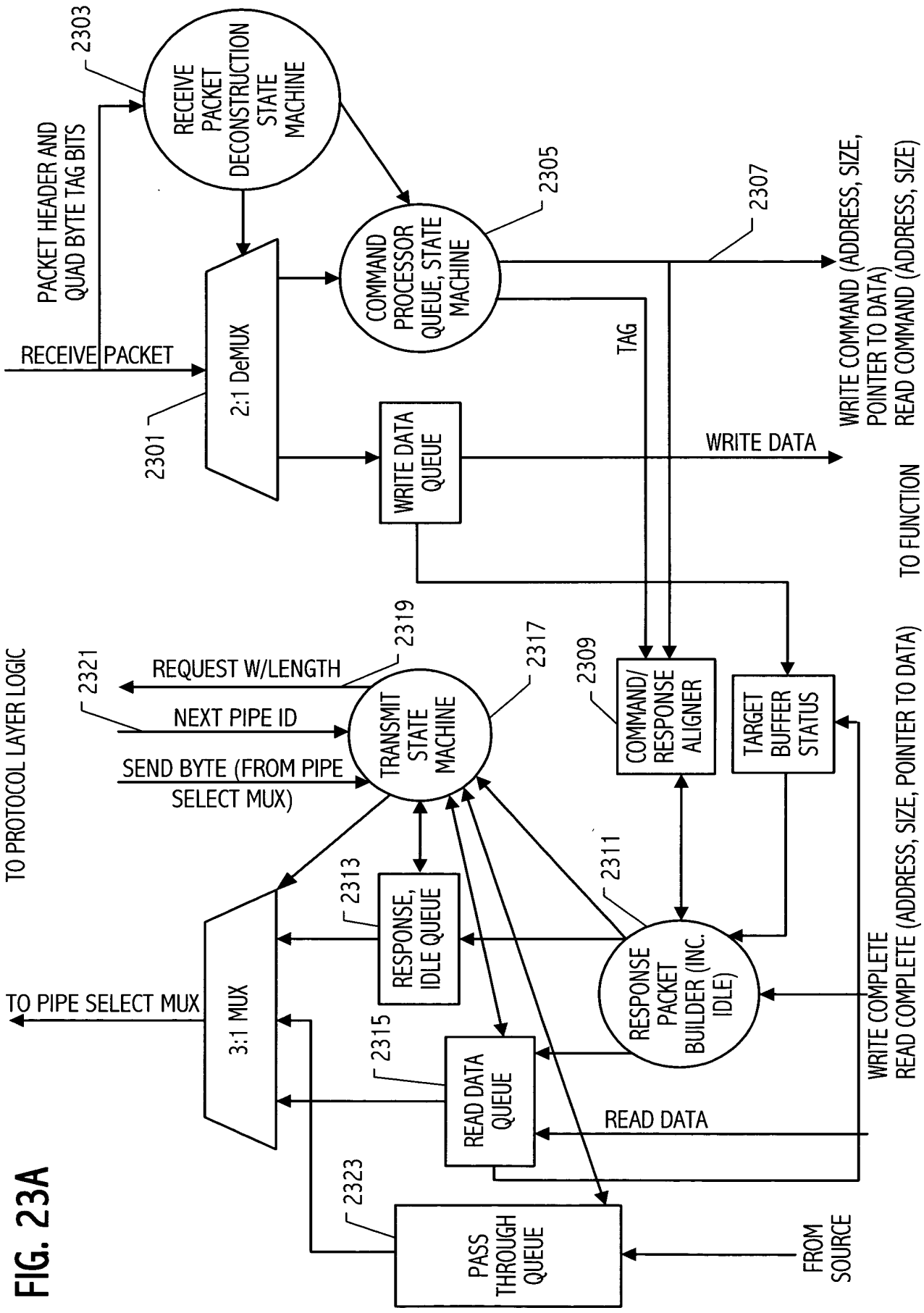
2303
RECEIVE PACKET DECONSTRUCTION STATE MACHINE
PACKET HEADER AND QUAD BYTE TAG BITS
RECEIVE PACKET
2301
2:1 DeMUX
2305
COMMAND PROCESSOR QUEUE, STATE MACHINE
2307
TAG
WRITE DATA QUEUE
WRITE DATA
WRITE COMMAND (ADDRESS, SIZE, POINTER TO DATA)
READ COMMAND (ADDRESS, SIZE)
TO FUNCTION
TO PROTOCOL LAYER LOGIC
2321
REQUEST W/LENGTH
NEXT PIPE ID
SEND BYTE (FROM PIPE SELECT MUX)
2319
TRANSMIT STATE MACHINE
2317
2309
COMMAND/ RESPONSE ALIGNER
TARGET BUFFER STATUS
2313
RESPONSE, IDLE QUEUE
2311
RESPONSE PACKET BUILDER (INC. IDLE)
TO PIPE SELECT MUX
3:1 MUX
2315
READ DATA QUEUE
READ DATA
WRITE COMPLETE
READ COMPLETE (ADDRESS, SIZE, POINTER TO DATA)
2323
PASS THROUGH QUEUE
FROM SOURCE

FIG. 23A

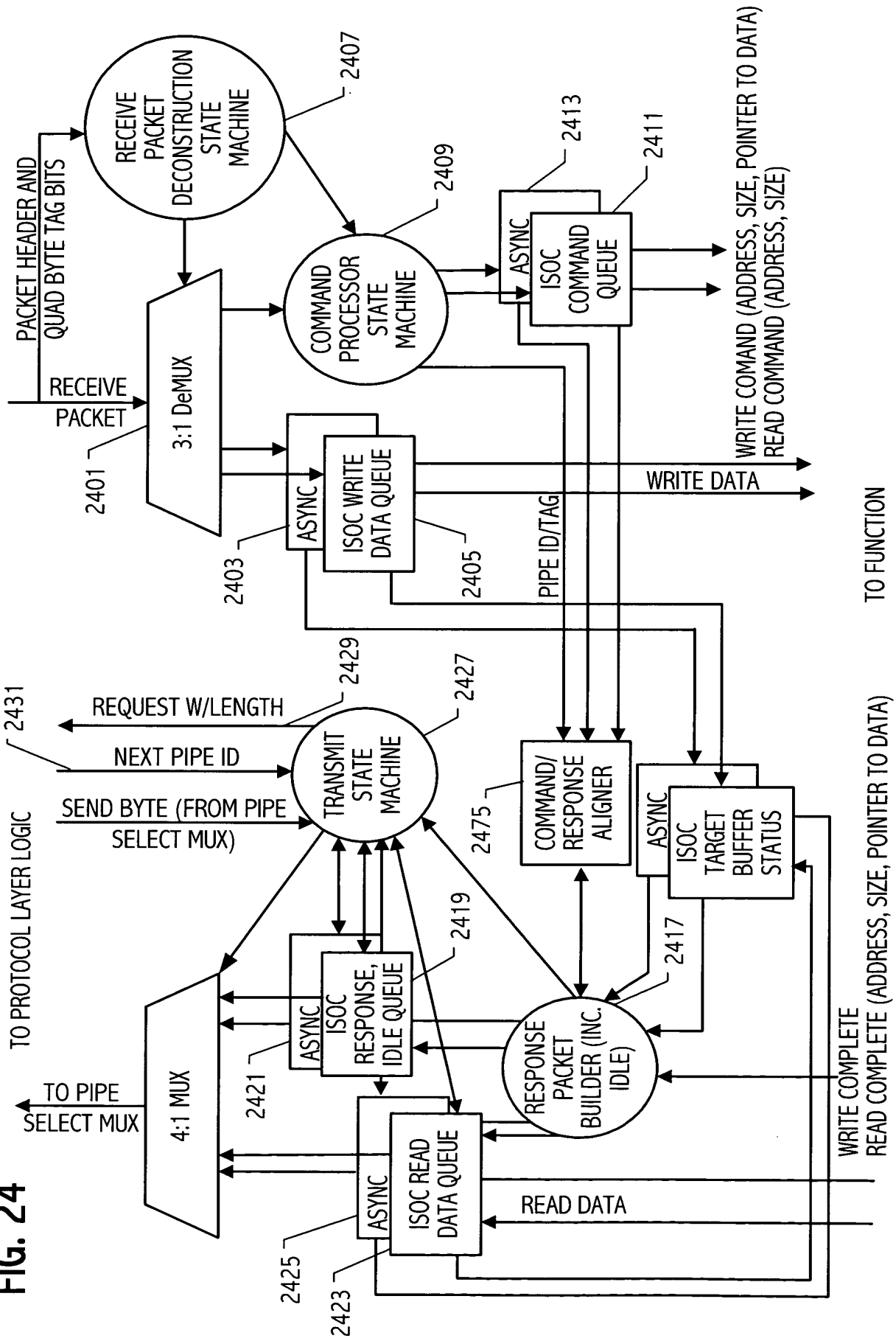
RECEIVE PACKET DECONSTRUCTION STATE MACHINE
2407
PACKET HEADER AND QUAD BYTE TAG BITS
RECEIVE PACKET
2401
3:1 DeMUX
COMMAND PROCESSOR STATE MACHINE
2409
ASYNC
ISOC COMMAND QUEUE
2413
2411
WRITE COMAND (ADDRESS, SIZE, POINTER TO DATA)
READ COMMAND (ADDRESS, SIZE)
ASYNC
ISOC WRITE DATA QUEUE
2403
2405
WRITE DATA
PIPE ID/TAG
TO FUNCTION
2431
REQUEST W/LENGTH
NEXT PIPE ID
SEND BYTE (FROM PIPE SELECT MUX)
TRANSMIT STATE MACHINE
2429
2427
COMMAND/ RESPONSE ALIGNER
2475
ASYNC
ISOC TARGET BUFFER STATUS
TO PROTOCOL LAYER LOGIC
2419
2417
ASYNC
ISOC RESPONSE, IDLE QUEUE
2421
RESPONSE PACKET BUILDER (INC. IDLE)
TO PIPE SELECT MUX
4:1 MUX
WRITE COMPLETE
READ COMPLETE (ADDRESS, SIZE, POINTER TO DATA)
ASYNC
ISOC READ DATA QUEUE
READ DATA
2425
2423

FIG. 24

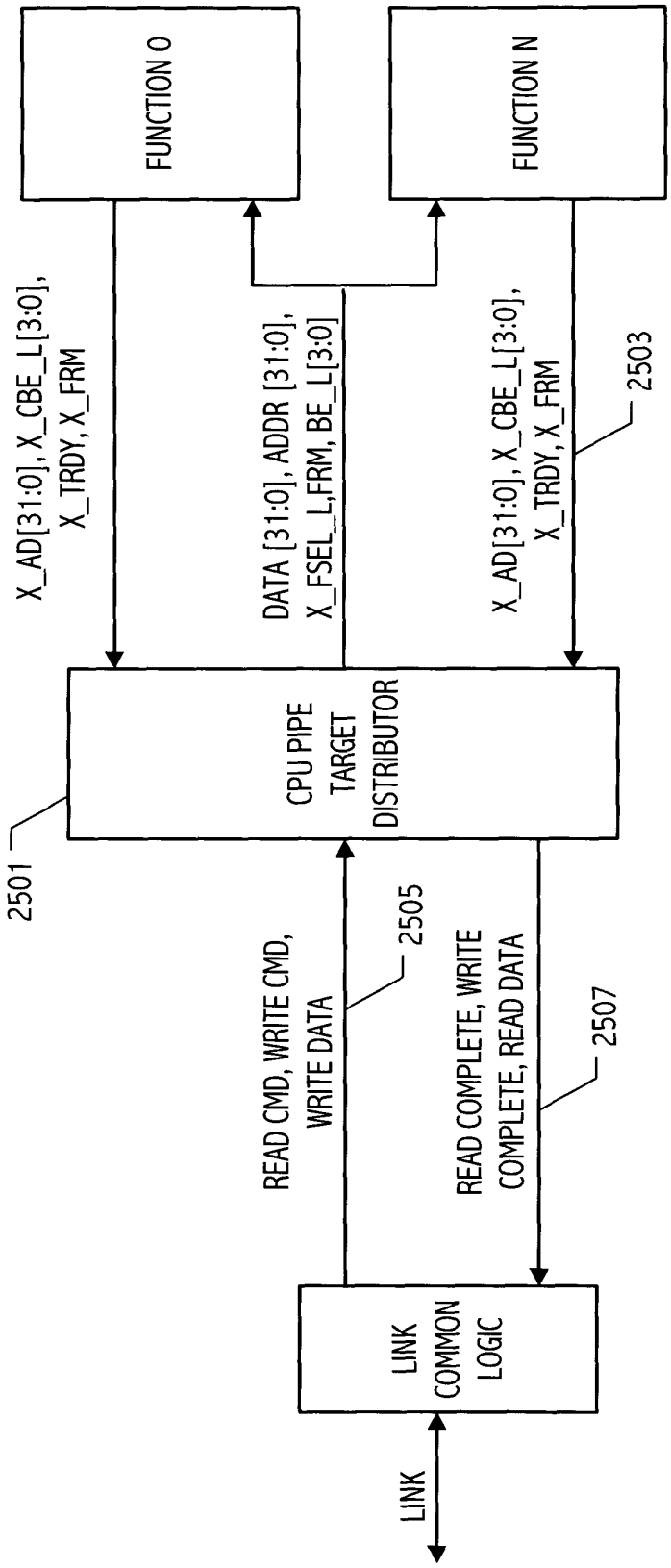
FUNCTION 0
FUNCTION N
X_AD[31:0], X_CBE_L[3:0], X_TRDY, X_FRM
DATA [31:0], ADDR [31:0], X_FSEL_L,FRM, BE_L[3:0]
X_AD[31:0], X_CBE_L[3:0], X_TRDY, X_FRM
2503
CPU PIPE TARGET DISTRIBUTOR
2501
READ CMD, WRITE CMD, WRITE DATA
2505
READ COMPLETE, WRITE COMPLETE, READ DATA
2507
LINK COMMON LOGIC
LINK

FIG. 25

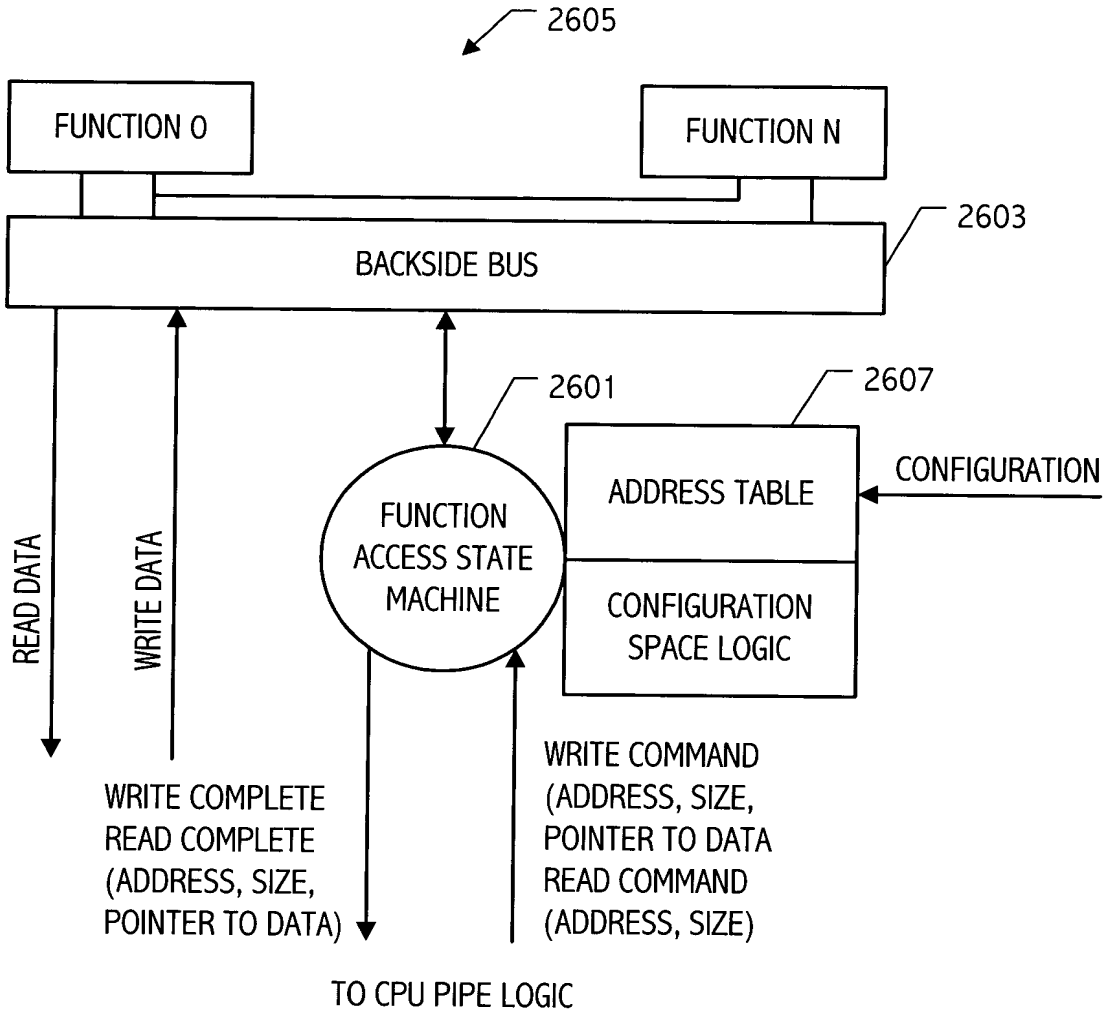
2605
FUNCTION 0
FUNCTION N
2603
BACKSIDE BUS
2601
2607
ADDRESS TABLE
CONFIGURATION
FUNCTION ACCESS STATE MACHINE
CONFIGURATION SPACE LOGIC
READ DATA
WRITE DATA
WRITE COMPLETE
READ COMPLETE
(ADDRESS, SIZE,
POINTER TO DATA)
WRITE COMMAND
(ADDRESS, SIZE,
POINTER TO DATA
READ COMMAND
(ADDRESS, SIZE)
TO CPU PIPE LOGIC

FIG. 26

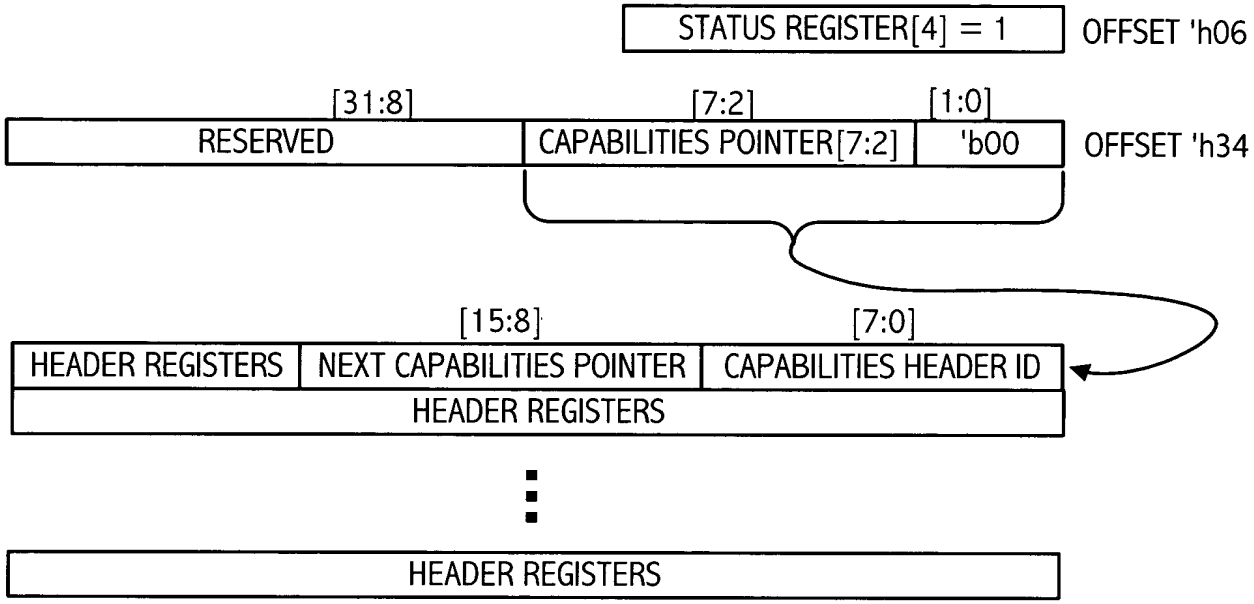
STATUS REGISTER[4] = 1
OFFSET 'h06
[31:8]
[7:2]
[1:0]
RESERVED
CAPABILITIES POINTER[7:2]
'b00
OFFSET 'h34
[15:8]
[7:0]
HEADER REGISTERS
NEXT CAPABILITIES POINTER
CAPABILITIES HEADER ID
HEADER REGISTERS
HEADER REGISTERS

FIG. 27

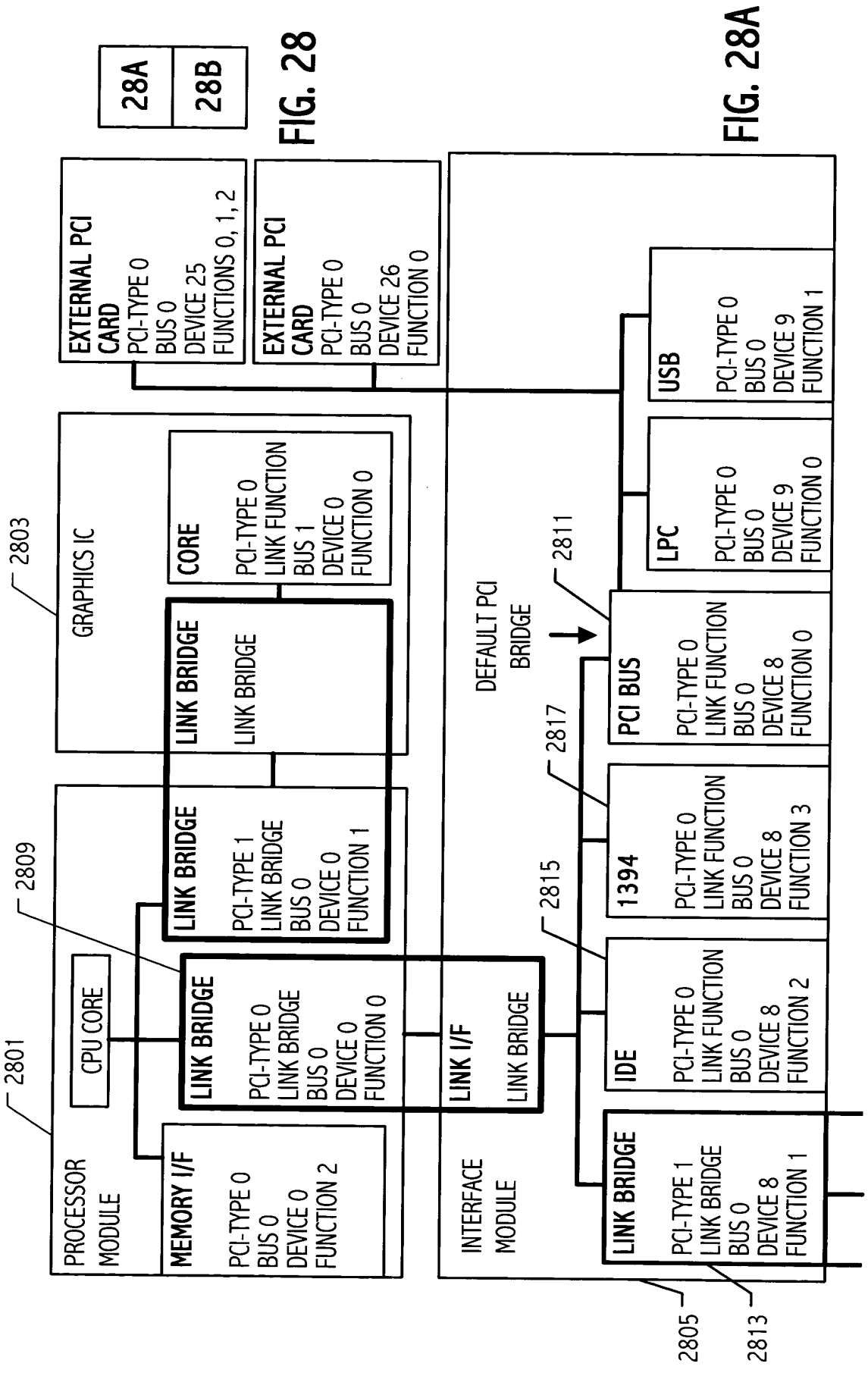

FIG. 28

FIG. 28A

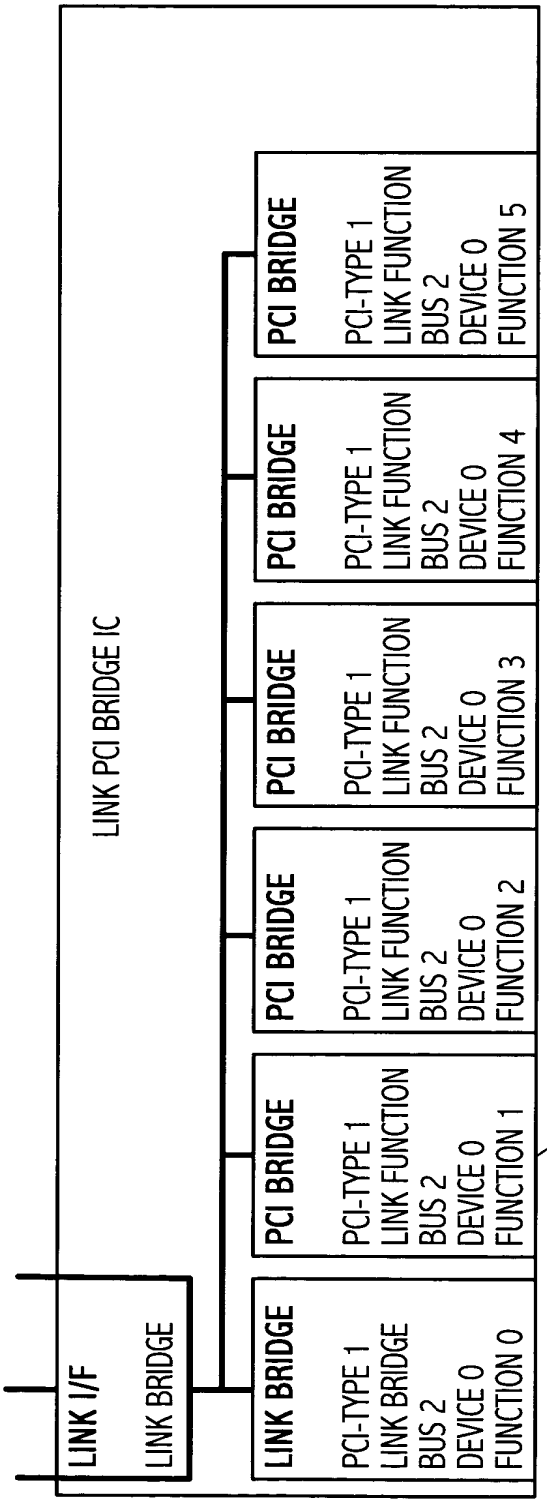
LINK PCI BRIDGE IC
LINK I/F
LINK BRIDGE
LINK BRIDGE
PCI-TYPE 1
LINK BRIDGE
BUS 2
DEVICE 0
FUNCTION 0
PCI BRIDGE
PCI-TYPE 1
LINK FUNCTION
BUS 2
DEVICE 0
FUNCTION 1
PCI BRIDGE
PCI-TYPE 1
LINK FUNCTION
BUS 2
DEVICE 0
FUNCTION 2
PCI BRIDGE
PCI-TYPE 1
LINK FUNCTION
BUS 2
DEVICE 0
FUNCTION 3
PCI BRIDGE
PCI-TYPE 1
LINK FUNCTION
BUS 2
DEVICE 0
FUNCTION 4
PCI BRIDGE
PCI-TYPE 1
LINK FUNCTION
BUS 2
DEVICE 0
FUNCTION 5
2807

FIG. 28B

TYPE 1

DEVICE ID		VENDOR ID		00h
STATUS		COMMAND		04h
CLASS CODE			REVISION ID	08h
BIST	HEADER TYPE	LATENCY TIMER	CACHE LINE SIZE	0Ch
BASE ADDRESS REGISTERS				10h 14h
SECONDARY LATENCY TIMER	SUBORDINATE BUS NUMBER	SECONDARY BUS NUMBER	PRIMARY BUS NUMBER	18h
SECONDARY STATUS		I/O LIMIT	I/O BASE	1Ch
MEMORY LIMIT		MEMORY BASE		20h
PREFETCHABLE MEMORY LIMIT		PREFETCHABLE MEMORY BASE		24h
PREFETCHABLE BASE UPPER 32 BITS				28h
PREFETCHABLE LIMIT UPPER 32 BITS				2Ch
I/O LIMIT UPPER 16 BITS		I/O BASE UPPER 16 BITS		30h
RESERVED			CAPABILITIES POINTER	34h
RESERVED				34h
EXPANSION ROM BASE ADDRESS				38h
BRIDGE CONTROL		INTERRUPT PIN	INTERRUPT LINE	3Ch

FIG. 29

PCI TYPE 0

DEVICE ID		VENDOR ID		00h
STATUS		COMMAND		04h
CLASS CODE			REVISION ID	08h
BIST	HEADER TYPE	LATENCY TIMER	CACHE LINE SIZE	0Ch
BASE ADDRESS REGISTERS				10h 14h 18h 1Ch 20h 24h
CARDBUS CIS POINTER				28h
SUBSYSTEM ID		SUBSYSTEM VENDOR ID		2Ch
EXPANSION ROM BASE ADDRESS				30h
RESERVED			CAPABILITIES POINTER	34h
RESERVED				38h
Max_Lat	Min_Gnt	INTERRUPT PIN	INTERRUPT LINE	3Ch

FIG. 30

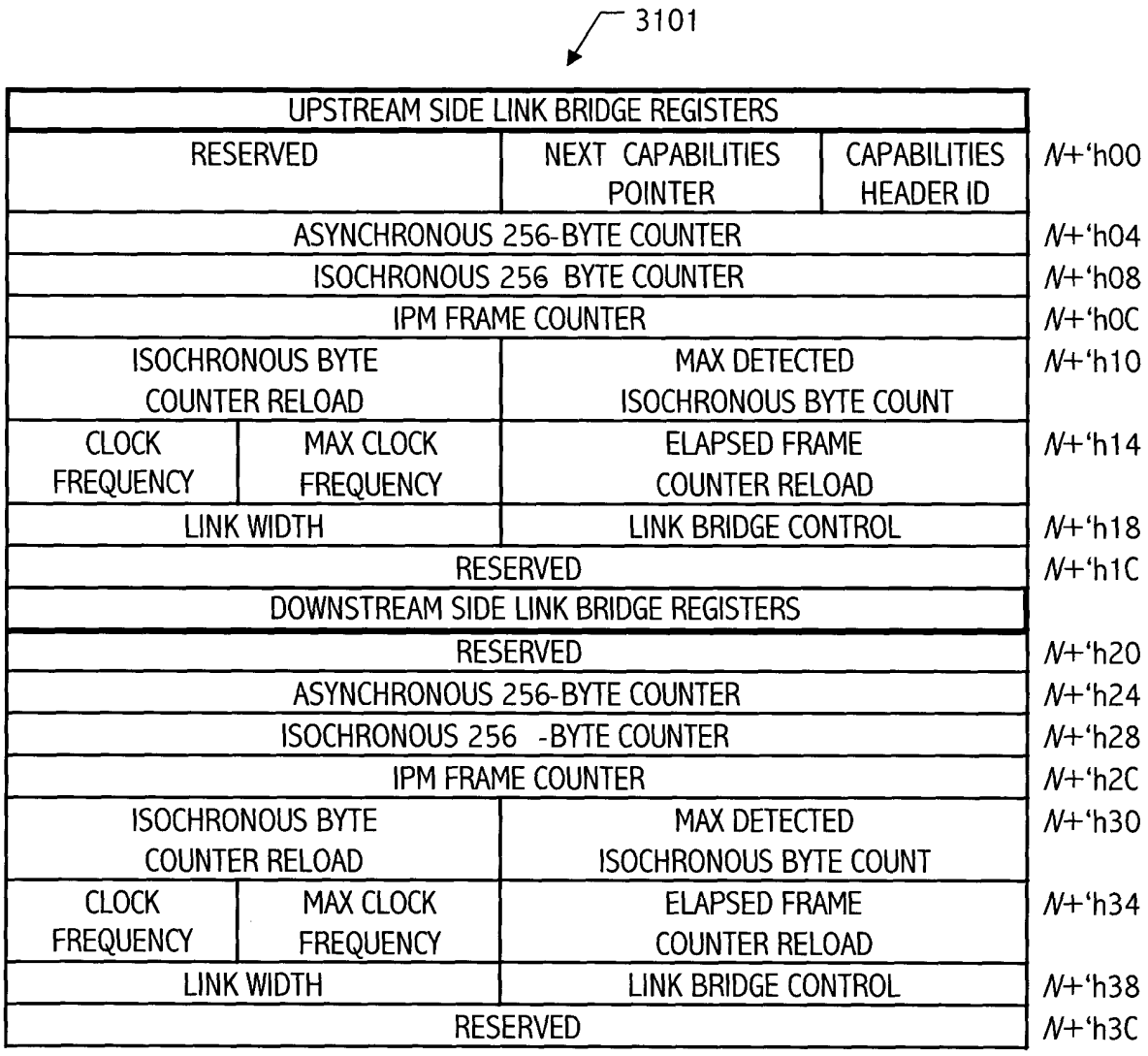
3101
UPSTREAM SIDE LINK BRIDGE REGISTERS
RESERVED
NEXT CAPABILITIES POINTER
CAPABILITIES HEADER ID
N+'h00
ASYNCHRONOUS 256-BYTE COUNTER
N+'h04
ISOCHRONOUS 256 BYTE COUNTER
N+'h08
IPM FRAME COUNTER
N+'h0C
ISOCHRONOUS BYTE COUNTER RELOAD
MAX DETECTED ISOCHRONOUS BYTE COUNT
N+'h10
CLOCK FREQUENCY
MAX CLOCK FREQUENCY
ELAPSED FRAME COUNTER RELOAD
N+'h14
LINK WIDTH
LINK BRIDGE CONTROL
N+'h18
RESERVED
N+'h1C
DOWNSTREAM SIDE LINK BRIDGE REGISTERS
RESERVED
N+'h20
ASYNCHRONOUS 256-BYTE COUNTER
N+'h24
ISOCHRONOUS 256 -BYTE COUNTER
N+'h28
IPM FRAME COUNTER
N+'h2C
ISOCHRONOUS BYTE COUNTER RELOAD
MAX DETECTED ISOCHRONOUS BYTE COUNT
N+'h30
CLOCK FREQUENCY
MAX CLOCK FREQUENCY
ELAPSED FRAME COUNTER RELOAD
N+'h34
LINK WIDTH
LINK BRIDGE CONTROL
N+'h38
RESERVED
N+'h3C
3102

FIG. 31